SIDDHARTH GROUP OF INSTITUTIONS :: PUTTUR
Siddharth Nagar, Narayanavanam Road – 517583

QUESTION BANK (DESCRIPTIVE)

Subject with Code : LDIC(13A03701) **Course & Branch**: B.Tech - EEE **Year & Sem:** IV-B.Tech & I-Sem **Regulation:** R13

UNIT –1

OP-AMP CHARACTERISTICS

1. Draw and explain the equivalent circuit of an operational amplifier. Give its features 10M
2. Draw the circuit diagram of an instrumentation amplifier using op-amp with its operation and derive the necessary expression 10M
3. (a) Suggest different methods to increase the input resistance of an op-amp. 10M
   (b)What are the features of IC 741?
4. Explain in detail all the DC and AC characteristics of an ideal OP-AMP with relevant expressions 10M
5. With neat circuit diagram explain the working principle of IC 723 voltage regulator 10M
6. What is an ideal active integrator? Explain its working with neat circuit diagram. 10M
7. Draw the circuit and explain the working of 10M
   (a) Voltage to current converter
   (b) Current to voltage converter
8. (a)List the characteristics of an ideal operational amplifier. 10M
   (b) What is frequency compensation and why is it required in operational amplifier? 10M

   10M
9. Draw the circuit diagram of Differentiator using op-amp and explain its operation with relevant wave forms 10M

10. a) What is op-amp?
2M
b) List out the ideal characteristics of op-amp
2M
c) What are the different kinds of packages of IC 741
2M
d) What are the assumptions made from ideal op-amp characteristics?
2M
e) Draw the pin configuration of IC741
2M

Unit-2
TIMERS, PHASE LOCKED LOOPS & D-A AND A-D CONVERTERS

1. With the aid of functional schematic diagram of 555 timer, explain how it can be used as astable multivibrator.
10M
2. (a) Explain the function of each pin of IC555 timer.
10M
(b) Draw the block diagram of IC565 and explain its operation.
10M
3. (a) Draw and explain the circuit diagram of parallel comparator type ADC.
10M
(b) Draw and explain the circuit operation of an inverted R-2R DAC.
10M
4. With the help of schematic diagram of 555 timer, explain how it can be used as mono stablemultivibrator
10M
5. (a) Draw the block schematic of PLL and explain the operation of each block
10M
(b) List the applications of PLL.
6. (a) Draw and explain the circuit diagram of dual slope ADC
10M
(b) Draw and explain the internal architecture of IC 1408 DAC
7. (a) What are the limitations of weighted resistor type D/A converter?
10M
(b) With neat block diagram, explain successive approximation type A/D converter in detail

8. Draw the circuit diagram of Schmitt trigger using op-amp and explain its operation withrelevant waveforms.
   10M
9. Draw the circuit of Schmitt trigger using IC555 timer and explain its operation?
   10M

10. a.What is a Schmitttrigger
    2M

    b.What is a bistable multivibrator
    2M

    c.Explain in brief the principle of operation of successive Approximation ADC
    2M

    d.Write the applications of V-I Converter
    2M

    e. Explain in brief stability of a converter
    2M

Unit-3
ACTIVE FILTERS & OSCILLATORS:

1. Design a first -order low pass filter so that it has a cut off frequency of 2kHz and pass Band gain of '1'.
   10M
2. Draw the circuit of a triangular-wave generator; explain its operation and derive expressions for frequency of oscillations?
   10M

3. Design Wien bridge oscillator using op-amp and derive the necessary expression. 10M
4. (a) Write notes on all pass filters. 10M
   (a) Write notes on VCO
5. Design and draw the triangular waveform generator using op-amp and explain its operation. 10M
6. Design RC phase shift oscillator using op-amp and derive the necessary expression. 10M
7. Design quadrature type oscillator using op-amp and derive the necessary expression. 10M
8. Design and draw the square wave generator using op-amp and explain its operation. 10M
9. Design and draw the saw tooth wave generator using op-amp and explain its operation. 10M

10.a. Mention few advantages of filters 2M

b.Draw the circuit for first order LPF filter using op-am 2M

c.Define an oscillator. What are the types of oscillators based on feedback used. 2M

d.Define BPF and write the expression for voltage gain 2M

e.Draw the circuit for first order HPF filter using op-amp 2M

UNIT-4
INTIGRATED CIRCUITS

1. (a) List out the merits and limitations of integrated circuit technology?
   10M
   (b) With suitable example, explain how CMOS logic driving by TTL logic
   10M
2. Perform the analysis of standard TTL NAND gate and give its characteristics
   10M
3. Explain the concept of MOS & CMOS open drain and tri-state outputs.
   10M
4. Explain the different variations came in chip size and circuit complexity.
   10M
5. Explain about TTL open collector outputs.
   10M
6. Define Moore's law and explain different classifications of integrated circuits.
   10M
7. Give the classification of integrated circuits and compare the various logic families.
   10M
8. What is meant by Tristate logic? Draw the circuit of Tristate TTL logic and explain the functions.
   10M
9. (a) List out the advantages of CMOS logic
   10M
   (b) Explain the concept of CMOS transmission gate.

10. a.What are the classifications of integrated circuits
    2M
    b.Write any two comparisons of all the logic families
    2M
    c.What are the stages in TTL NAND gate structure
    2M
    d.Write few characteristics of TTL NAND gate
    2M

e.Draw the structure of open collector output with pull-up resistor
2M

UNIT-5
COMBINATIONAL &SEQUENTIAL CIRCUITS

1. (a) Construct a full adder circuit using two half adders and basic logic gates.
   10M
   (b) Draw the circuit diagram of a 4-bit ripple carry adder using 4 full adder circuit blocks.
2. (a) Explain with suitable example how binary multiplication can be performed using shift and add method?
   10M
   (b) Design and draw the circuit diagram of decade counter and explain its operation
3. (a) With the help of logic diagram of a 4-bit adder/subtractor for adding or subtracting two numbers of arbitrary signs, using 1's complement and explain its working?
   10M
   (b) Design a 4-bit parallel full adder with look ahead carry scheme?
4. (a) Design a 3 input 5-bit multiplexer? Write the truth table and draw the logic diagram? 10M
   (b) Design a full subtractor with logic gates?

5. (a) Give the design considerations of 2×4 decoder and explain the operation with relevant circuit Design a parallel binary adder circuit using 2's complement system.
   10M
   (b) Design a 4-bit bidirectional shift register with parallel load
6. (a)Write short notes on Ring Counter and Johnson counter.
   10M
   (b) Design a conversion circuit to convert a D flip-flop to J-K flip-flop?
7. (a) Give the design considerations of parity encoder and explain the operation with relevant circuit.
   10M
   (b) Design a parallel binary subtractor circuit using 2' s complement system.
8. Write short notes on the following:
   10M
   a. Level triggering.
   b. Edge triggering.
   c. Pulse triggering
   d. Explain the RS flip-flop using NAND gates?
9. (a) Design a conversion circuit to convert a D flip-flop to J-K flip-flop?
   10M
   (b) What is meant by a transparent latch?

10. a.What are the different types of code converters
    2M
    b.Define decoder and encoder
    2M
    c.Define mux and demux
    2M
    d.Draw the pin configuration of decoder used for driving LED and LCD display
    2M.
    e.Define priority encoder and its significance
    2M

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QUESTION BANK (OBJECTIVE)

Subject with Code : LDIC(**13A04508**) **Course & Branch**: B.Tech – EEE
Year & Sem: III-B.Tech & I-Sem **Regulation:** R13

UNIT-1
OP-AMP CHARACTERISTICS

1. IC-741 op-amp has typical gain of in dB [ ]

(a) 110 dB (b) 100 dB (c) 106 dB (d) 90 dB

2. Ideal terminal conditions of IC-op-amp are [ ]

(a) $V_d = \infty$, $V_0 = 0$,. $i_P = i_N = 0$. (b) $V_d = 0$, $V_0 = \infty$, $i_p = i_N = \infty$
(c) $V_d = 0$, $V_0 = 0$, $i_P = 0$, $i_{N=} \infty$ (d) $V_d = 0$, $V_0 = 0$, $i_P = \infty$, $i_{N=0}$

3.The differential mode and common mode voltage is defined as [ ]

(a) $V_{DM} = V_2 - V_1$, $V_{CM} = V_1 + V_2/2$ (b) $V_{DM} = V_1 + V_2/2$, $V_{CM} = V_2 - V_1$
(c) $V_{DM} = V_1/_2 = V_2/_2$, $V_{CM} = V_2 - V_1/_2$ (d) none of the above

4.The ideal input impedance range of op-amp is [ ]

(a) 1 kΩ (b) 10 kΩ to 10^6 mΩ (c) 10^6 mΩ to 10^{12} mΩ (d).None

5.Which of the following amplifier compensates for drift? [ ]

(a) Low gain amplifier (b) High gain amplifier (c) DC amplifier
(d) Differential amplifier

6.An ideal amplifier should have [ ]

(a) infinite gain at all frequencies (b) large bandwidth (c) zero phase shift (d) all of the above

7.An amplifier is an unstable condition when [ ]

(a) gain is low (b) load is variable (c) phase shift is 180° (d) supply is rectified DC

8.Noise in op-amp can be reduced to [ ]

(a) shielding (b) use lpf (c) proper grounding (d) all of the above

9. A _____amplifier amplifies the difference between two input signals. [ ]
(a) Differential amp (b) Inverting amp (c) Non Inverting amp(d) none

10.The second state of OP_AMP consists of dual input ------- output

differential amplifier. [ ]
(a) Balanced (b) Unbalanced (c) Single (d) dual
11.A monolithic circuit means [ ]

(a) circuit from single crystal (b) circuit from more than one crystal
(c) uses double price of crystal to form a circuit (d) none of the above

12.The CMRR of MA 741 is [ ]

(a) 70 db (b) 50 db (c) 40 db (d) none
13.The basic elements of op-amp is [ ]

(a) differential amplifier (b) buffer, level translator (c) output driver
(d) all of the above
14.Differential gain can be expressed as [ ]

(a) A_d= Vo/Vd (b) A_d= Vo/Vd (c) A_d= Vo/Vd (d) none
15. For an ideal differential amplifier, the differential gain must be_____ while common mode gain must be__ [ ]
(a) zero, infinite (b) infinite, infinite (c) zero, zero (d) infinite, zero
16.Common mode rejection ratio can be expressed as [ ]

(a) CMRR= Ac/Ad (b) CMRR= Ad/Ac (c) CMRR= Vc/Vd (d) CMRR= Vd/Vc
17. The differential amplifier can be operated in____ [ ]

(a) Differential mode (b) Common mode (c) Both (d) none
18. DC character of op-amp are [ ]

(a) input bias and offset current (b) input offset voltage (c) thermal drift
(d) all of the above
19. A current mirror can be used as an active load because it has [ ]
(a) low resistance (b) high ac resistance (c) low ac resistance (d) high dc resistance
20.The slew rate for IC 741 is [ ]

(a) 0.5 V/μs (b) 0.9 V/μs (c) 0.8 V/μs (d) 1 V/μs
21.Op-amp 741C cannot be used for high frequency applications because [ ]
(a) low slew rate (b) high slew rate
22.DC analysis means to obtain the operating values of [ ]

(a) Icq and Vce (b) Ibq and Vbe (c) Icq and Vbe (d) none
(c) O.T. V/QS (d) none of the above

23. AC analysis of Differential amplifier can be find using__ [ ]

(a) h-parameters (b) r-parameters (c)both (d) z-parameters

24. Differential amplifier is ----------coupled amplifier [ ]

(a) emitter (b) direct (c)cascode (d) none

25. Level shifter of op-amp should have ----------input impedance [ ]

(a) zero (b) infinite (c)not defined (d) none

26. Military grade op-amp be operated in the temperature range of [ ]

(a) − 55 to 120°C (b) − 50 to 150°C (c) 0 to 100°C (c) at 30°C

27. The reason for op-amp to drive any number of input devices corrected to its output is

(a) zero output resistance (b) infinite output resistance [ ]

(c) high output resistance (d) none

28. Open loop operation of op-amp has output [ ]

(a) + V_{sat} (b) − V_{sat} (c) − V_{sat}, − V_{sat} (d) V_{sat} = 0

29. The input offset voltage of the practical Op-amp in the order of the __[ ]

(a) 1mV (b) 10mV (c) 100mV (d) none

30. Input impedance of DIBO-DA is_____ [ ]

(a) $2\beta_{ac}r_e$ (b) $2\beta_{ac} / r_e$ (c) $\beta_{ac}r_e$ (d) β_{ac} / r_e

31.Voltage gain of SIBO-DA is_____. [ ]

(a) $R_c / 2r_e$ (b) $R_c \times 2r_e$ (c) R_c / r_e (d) $R_c \times r_e$

32. level shifter is used to bring DC level down to_____ level [ ]

(a) zero (b) infinite (c) not possible (d) none

33. Open loop operation of op-amp has output [ ]

(a) zero (b) infinite (c)not defined (d) none

34. Voltage gain of DIBO-DA is_____ [ ]

(a) $R_c / 2r_e$ (b) $R_c \times 2r_e$ (c) R_c / r_e (d) $R_c \times r_e$

35. For large CMRR, A_{CM} should be [ ]

(a) High (b) Low (c) Both (d) Not defined

36. The gain of an op-amp decreases at high frequency due to [ ]

(a) Input offset voltage (b) bias current (c) slew rate (d) none

37. The input bias current of the practical Op-amp in the order of the ___ [ ]

(a) 40nA (b) 60nA (c) 80nA (d) none

38. A differential amplifier amplifies the ---------- between two input signals. [ ]

a) addition b) subtraction c) multiplication d) both b and c

39. Noise of input signal in differential amplifier [ ]

a) increases b) decreases c) remains the soul d) none

40. Cascaded differential amplifier requires level translator because of [ ]

a) impedance matching b) isolating each stage c) d.c.shift d) none

UNIT-2
TIMERS, PHASE LOCKED LOOPS & D-A AND A-D CONVERTERS

1. The duty cycle of a symmetric square worm of astable is [ ]

A). $R_B/(R_A+R_B)$ B). $R_A/(R_A+2R_B)$ C). $R_B/(R_A+2R_B)$ D). none

2. The out put frequency of a symmetric square worm of astable is [ ]

A). $1.45/(R_A+2R_B)C$ B). $1.45/(R_A+R_B)C$ C). $1.45/(R_A-R_B)C$ D). none

3. Voltage to frequency conversion factor K_v of a VCO is defined as [ ]

A). $\Delta Vc/\Delta fo$ B). $\Delta Vc.\ \Delta fo$ C). $\Delta fo/\Delta Vc$ D). $\Delta Vc+\Delta fo$

4. Voltage to frequency conversion factor K_v of a VCO is [ ]

A). 6fo/Vcc B). 7fo/Vcc C). 8fo/Vcc D). none

5. Which Multivibrator does not require a input (Clock pulse or other). [ ]

A) Monostable MV B) Bistable MV C) ASTABLE MV D) ALL

6.The output frequency of a FSk generator is [ ]

A). 1070-1200 Hz B). 1070-1270 Hz C). 1000-1270 Hz D).none

7. The duty cycle of a symmetric square worm is [ ]

A). 25% B). 50% C). 75% D).100%

8. The V_{LTP} and U_{LTP} OF Schmitt trigger is [ ]

A). 1/3Vcc,1/2Vcc B). 2/3Vcc,1/2Vcc C). 1/3Vcc,2/3Vcc D). none

9. Application of monostable multivibrator is [ ]

A). PWM B). Linear ramp C). frequency divider D).all

10. _____is applied to make the output is voltage is zero [ ]

A). Threshold B). Discharge C). reset D).all

11._____multivibrator having two quasi stable states [ ]

A). astable B). mono stable C). bistable D).none

12._____ detector I better capture and locking characteristics as the DC outpt voltagae iss linear up to 360º [ ]

A). X-OR B). RS flip flop C). both D). none

13. Which one is true in the locking or tracking range [ ]

A). fs = fo B). fs ± fo C). fs /fo D). all

14. Applications of PLL are [ ]

A). Freq multiplication B). Freq translation C). AM detection D). all

15. The error voltage for analog phase detector Ve is [ ]

A). $K_\varphi(\varphi-\pi)$ B). $K_\varphi/(\varphi-\pi)$ C). $K_\varphi(\varphi-\pi/2)$ D). $K_\varphi/(\varphi-\pi)$

16. The pulse width of the mono stable multivibrator is [ ]

A). 0.69RC B). 0.45RC C). 1.1 RC D). none

17.The output frequency fo of VCO is given by [ ]

A).$0.25/R_T C_T$ B). $0.5/R_T C_T$ C). $1/R_T C_T$ D). none

18. Conversion ratio o f the phase detector of 565IC PLL is $K_Ø$ = [ ]

A).0.7/Π B). 0.3/Π C). 1.4/Π D). 0.6/Π

19.The phase shift φ should be inn locked state is [ ]

A). 90º B). 180º C). 270º D). 360º

20. At what phase angle of φ the fo should deviate from centre to the right side in proportional to the error voltage [ ]

A). 0º B). 180º C). 270º D). 90º

21. At what phase angle of φ the fo should deviate from Centre to the right side in proportional to the error voltage [ ]

A). 0º B). 180º C). 270º D). 90º

22. The output frequency of the phase detector is [ ]

A). sum B). difference C). both A&B D). 90º

23._____ logic gate is used to perform the digital phase detection [ ]

A). nand B). nor C). X-NOR D). X-OR

24.The output of Schmitt trigger is [ ]

(a) square waveform (b) triangular waveform (c) sine waveform (d) cos waveform

25.The other name of Schmitt trigger is [ ]

(a) regenerative comparator (b) square wave generator (c) backlash circuit (d) all

26.The total time period of the pulse from monostable multivibrator is [ ]

(a) T = 2 RC (b) T = 0.3 RC (c) T = 0.69 RC (d) T = RC ln (1 + V_D/V_{sat})/$_1-\beta$

27.The single output pulse of adjustable time direction in response to triggering signal is from _____ circuit. [ ]

(a) astable multi (b) monostable multi (c) bistable multi (d) none

28.The other name of astable multivibrator is [ ]

(a) Schmitt trigger (b) free running oscillator (c) regenerative comparator (d) none

29.The frequency of oscillation of triangular waveform from generator using op-amp

(a) $R_3/4R_1C_1R_2$ (b) $R_2/4R_1C_1R_3$ (c) $R_1/4R_3C_1R_2$ (d) none [ ]

30.A comparator is _____ and gives _____ output. [ ]

(a) Open loop op-amp, Analog output (b) Open loop op-amp, No output

(c) Open loop op-amp, Digital output (d) Closed loop op-amp, Digital output

31.Schmitt trigger is comparator _____ feedback. [ ]

(a) no feedback (b) positive feedback (c) negative feedback (d) none

32.A triangular wave can be generated by integrating [ ]

(a) cosine waveform (b) sine waveform (c) ramp waveform (d) square waveform

33.The application of open-loop operation of op-amp is [ ]

(a) zero crossing detector (b) square wave generator (c) comparator (d) all

34. The input offset voltage of the practical Op-amp in the order of the __[ ]

(a) 1mV (b) 10mV (c) 100mV (d) none

35. The gain of an instrumentation amplifier is varied by a single_____ [ ]

(a) Resistor (b) Capacitor (c) Inductor (d) all

36. An Op-amp current to voltage converter is also called as_____ [ ]

(a) Current amp (b) voltage amp (c) frequency amp (d) none

37. An active integrator may be used to convert a square wave into a_____wave

(a) sine (b) cos (c) triangular (d) none [ ]

38.The application of op-amp in non-linear region is [ ]

(a) comparators (b) detectors (c) limiters (d) all

39. The gain of the Inverting amplifier is_____ [ ]

(a) Acl = $-R_f \times R_i$ (b) $-R_f / R_i$ (c) $[1+R_f / R_i]$ (d) $[1+R_f / R_i]$

40. The gain of the Non inverting amplifier_____ [ ]

(a) Acl = $-R_f \times R_i$ (b) $-R_f / R_i$ (c) $[1+R_f / R_i]$ (d) $[1+R_f / R_i]$

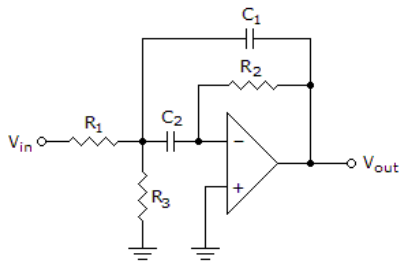
UNIT-3
ACTIVE FILTERS & OSCILLATORS

1. A _____ filter rejects all frequencies within a specified band and passes all those outside this band.
A. low-pass B. High pass C. band pass D. band stop [ ]

2. Filters with the _____ characteristic are useful when a rapid roll-off is required because it provides a roll-off rate greater than –20/dB/decade/pole.
a. Butterworth b. Chebyshev c. Bessel d. none [ ]

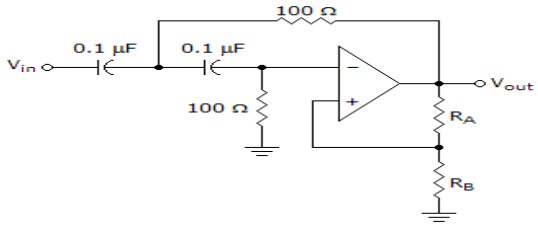
3. A _____ filter significantly attenuates all frequencies below f_c and passes all frequencies above f_c.
A. low-pass B. High pass C. band pass D. band stop [ ]

4. The gain of the multiple-feedback band-pass filter above is equal to which of the following? Assume $C = C_1 = C_2$.



a. $A_0 = R_2 / R_1$ b. $A_0 = R_1 / R_2$ c. $A_0 = R_2 / 2R_1$ d. $A_0 = R_1 / R_2$ [ ]

5. Refer to the given figure. This circuit is known as a _____ filter, and the f_c is [ ]



a. high-pass, 1.59 kHz b. band-pass, 15.9 kHz c. low-pass, 15.9 kHz d. high-pass, 15.9 kHz

6. The bandwidth in a _____ filter equals the critical frequency [ ]
a. low-pass b. high-pass c. band-pass d. band-stop

7. Filters with the _____ characteristic are used for filtering pulse waveforms
a. Butterworth b. Chebyshev c. Bessel d. none [ ]

8. The critical frequency is defined as the point at which the response drops _____ from the passband.
a. –20 dB b. –3 dB c. –6 dB d. –40 dB [ ]

9. Filters with the _____ characteristic provide a very flat amplitude in the passband and a roll-off rate of –20 dB/decade/pole.
a. Butterworth b. Chebyshev c. Bessel d. none [ ]

10. A low-pass filter has a cutoff frequency of 1.23 kHz. Determine the bandwidth of the filter
a. 2.46khz b. 1.23khz c. 644hz d. 123khz [ ]

11. One important application of a state-variable _____ filter with a summing amplifier is to minimize the 60 Hz "hum" in audio systems.

A. low-pass B. High pass C. band pass D. band stop [ ]

12. Only the condition βA = _____ must be satisfied for self-sustained oscillations to result.
a. 0 b. -1 c. 1 d. none [ ]

13. At what phase shift is the magnitude of βA at its maximum in the Nyquist plot?
a. 90º b. 270º c. 180º d. 0º [ ]

14. Which of the following improvements is (are) a result of the negative feedback in a circuit? [ ]
a. Lower output impedance b. Reduced noise c. More linear operation d. all

15. The feedback signal in a(n) _____ oscillator is derived from an inductive voltage divider in the LC circuit. [ ]
a. Hartley b. Armstrong c. colpits d. wien bridge

16. The attenuation of the three-section RC feedback phase-shift oscillator is [ ]
a. 1/9 b. 1/30 c. 1/3 d. 1/29

17. advantages of filters [ ]
a. reduction in size b. less cost c. easy tuning d. all of the above

18. types of oscillators based on circuit components [ ]
a. RC b. audio freq osci c. high freq osci d. feedback osci

19. in RC circuit voltage across resistance is of _____phase shift [ ]
a. 90º b. 270º c. 0º d. 180º

20. For a phase-shift oscillator, the gain of the amplifier stage must be greater than[ ]
a. 19 b. 29 c. 30 d. 1

21. Which of the following is (are) the determining factor(s) of the stability of a feedback amplifier? [ ]
a. Phase shift between input and output signals b. A
c. Both A and the phase shift between input and output signals d. none

22. What is the minimum frequency at which a crystal will oscillate? [ ]
a. 7^{th} harmonic b. third harmonic c. fundamental harmonic d.2^{nd} harmonic

23. An amplifier with a gain of –500 and a feedback of β = –0.1 has a gain change of 15% due to temperature. Calculate the change in gain of the feedback amplifier. [ ]
a.0.2% b. 0.3% c. 0.4% d. 0.5%

24. the RC feedback network produces a phase shift of [ ]
a. 90º b. 270º c. 0º d. 180º

25. quadrature oscillator has a phase shift of [ ]
a. 90º b. 270º c. 0º d. 180º

26. triangular wave generator can be formed by cascading [ ]
a. integrator-differentiator b. integrator-square wage g/r
c. square wage g/r- integrator d. differentiator-integrator

27. sawtooth wave forms can be generated with little modifications in……. [ ]
a. sine b. square wave c. triangular d. cosine

28. which of the following has unequal rise and fall times [ ]
a. sawtooth b. sine c. square d. triangular

29. which of the following may fall negatively many times faster than it rises positively

a. sawtooth b. sine c. square d. triangular [ ]

30. which of the following classified as astable multi vibrator [ ]

a. sawtooth b. sine c. square d. triangular

31. an oscillator by which frequency of oscillations can be controlled by an externally applied voltage is called…….. [ ]

a. RC osci b. LC osci c. VCO d. wien bridge osci

32. The feedback signal in a(n) _____ oscillator is derived from a capacitive voltage divider in the LC circuit. [ ]

a. Hartley b. Armstrong c. colpits d. wien bridge

33. filters are classified as [ ]

a. active b. passive c. both a and b d. none

34. Which of the following is required for oscillation? [ ]

a. βA > 1 b. The phase shift around the feedback network must be 180º

C. both a and b d. none

35. A circuit that can change the frequency of oscillation with an application of a dc voltage is sometimes called [ ]

a. VCO B. hartely c. colpitts d. wien bridge

36. In order to start up, a feedback oscillator requires [ ]

a. negative feedback less than 1. b. positive feedback greater than 1. C.unity feedback equal to 1. D. no feedback.

37. What is the ratio of the input impedance with series feedback to that without feedback?

a. 1 + βA b. βA c. β d. 1 [ ]

38. Which of the following oscillators is (are) tuned oscillators? [ ]

a. hartely b. colpitts c. wien bridge d. all of the above

39. What is the ratio of the output impedance with series feedback to that without feedback?

a. 1 + βA b. βA c. β d. 1 [ ]

40. One condition for positive feedback is that the phase shift around the feedback loop must be _____°. [ ]

a. 90º b. 270º c. 0º d. 180º

UNIT-4
INTIGRATED CIRCUITS:

1. The range of Voh min in cmos circuit is [ ]
a) Vcc-0.7v b)Vcc-0.1v c) Vcc-0.6v d)Vcc-0.2v

2.Low output of TTL is in between [ ]
a)2 to 5 b)2 to 3 c)0 to 0.8 d)0 to 2

3.TTL output stage is called___ [ ]
a)Totempole b)Push back c)Pull back d)Pull down

4.In bipolar logic family____type of transistor operates fastly [ ]
a)Npn b)Pnp c)Schottky transistor d)Cc transistor

5.V-gamma voltage of Schottky transistor [ ]
a)0.25 b)0.6 c)0.3 d)0.4

6.The negative leakage current flow in diode when it is [ ]
a)Forward biased b)Reversed bias c)Short circuit d)Constant

7.In transistor logic family____region works as binary 1 [ ]
a)Cut off region b)Active region c)Saturation region
d)Break down region

8.We can also call transistor as _____diodes connected [ ]
a)Back to front b)Back to back C)Front to back d)Front to front

9.Basically the single stage CE transistor act as logic circuit [ ]
a)Multiplexer b)Inverter c)Differentiator d)Decoder

10.The 74F family is positioned between ___and ____in the speed/powertrade off [ ]
a)74S,74LS b)74LS, 74AS c)74S,74AS d)74AS,74ALS

11.The original TTL family of logic gates was introduced by ____in 1963 [ ]
a)Paul b)Leach c)Sylvania d)Goutham saha

12.Speed power product units used in 74ALS family [ ]
a)Ns b)Mw c)Pj d)V

13.Power consumption per gate units used in 74F family [ ]
a)Ns b)mw c)Pj d)Watts

14.More power consumption present from following family [ ]
a)74LS b)74AS c)74ALS d)74S

15.The value of IloLmax for typical LS TTL output is exactly ____times the absolute [ ]
a)10 b)20 c)40 d)5

16. The absolute value of IoHmax is exactly _____times I in LS-TTL [ ]
a)10 b)20 c)40 d)5

17.Best family of following according to speed power product [ ]
a)74S b)74LS c)74AS d)74ALS

18.Best family of following according to power consumption per gate [ ]
a)a74S b)74LS c)74AS d)74ALS

19.In _____transistors acts as a VCR [ ]

A. TTL, ECL B. CMOS, NMOS C. CMOS,TTL D. NMOS,TTL

20.In CMOS logic1 represents_____. [ ]

A. 0-1.5V B. 1.5-2.5V C. 3.5-5V D. 0-0.8V

21.In MOS transistor has very high impedance because the gate separates source and drain by an material with a very high resistance. [ ]

A. semiconductor B. insulator C. conductor D. wood

22.When current flows from the power supply out of the device output and through the load to ground. [ ]

A. sourcing current B. sinking current C. conventional current D. leakage current

23.In two input CMOS and gate no.of transistors used are [ ]

A. 4 B. 2 C. 8 D. 16

24. BJT is used as [ ]

A. voltage amplifier B. Current amplifier C. Switch D. all of the above

25.The value of I_{IHmax} in LS-TTL family [ ]

A. 10µA B. 20µA C. 40µA D. 10µA

26.The value of I_{ILmax} in LS-TTL family [ ]

A. 0.4mA B. -0.4mA C. 8mA D. -0.8mA

27.In TTL NAND gate, the diode circuit produces_____logic [ ]

A. AND B. NAND C. OR D. NOR

27.Germanium diodes have _____ cut-in voltage [ ]

A)0.7 B)0.3 C)0.25 D)0.6

28.In CMOS driving TTL the CMOS output V_{OH}(min) is _____ [ ]

A)4.95V B)3.45V C)0V D)2.59V

29. In CMOS driving TTL the CMOS output I_{OL}(max) is _____ [ ]

A)4.95mA B)0.45mA C)0.12mA D)2.59mA

30. In CMOS driving TTL the TTL output I_{IH}(max) is _____ [ ]

A)40uA B)0.45uA C)0.12uA D)2.59uA

31. In CMOS driving TTL the TTL output I_{IL}(max) is _____ [ ]

A)4.95mA B)1.6mA C)0.12mA D)2.59mA

32.The fastest Logic family is _____ [ ]

A)CMOS B)TTL C)DTL D)ECL

33. Integrated circuits are classified as [ ]

A. SSI B.MSI C.VLSI D. ALL OF THE ABOVE

34.chip size of ASIC in the year of 2014 interms of mm^2 is [ ]

A. 800 B. 1000 C. 1300 D. 1482

35. which of the following family is more vulnerable to noise [ ]

A. TTL B.ECL C.CMOS D.DTL

36. TTL NAND gate consists of [ ]

A. Phase shifter B. diode and gate C. both a and b D. envelope detector

37. open drain outputs are used primarily for [ ]

A. driving LED'S B. driving multi-source buses C. performing wired logic D. all

38. in driving LED'S $V_{OL(MAX)}$is [ ]

A. 0.37V B. 3.7V C. 1.5V D. 0.15V

39. Transmission gate is operated such that the signals EN and EN_L are at [ ]

A. LOW, LOW B. HIGH, LOW C. HIGH, HIGH D. both b and c

40. Relationship between TTL and CMOS for the parameter of voltage is [ ]

A. $V_{OH(MIN)} << V_{IH(MIN)}$ B. $V_{OH(MIN)} >> V_{IH(MIN)}$ C. $V_{OH(MIN)} == V_{IH(MIN)}$ D. none

UNIT-5
COMBINATIONAL &SEQUENTIAL CIRCUITS

1. For 74X139 dual 2 to 4 decoder,011 input gives _ _ _ _ _ _ output. [ ]
a. 1011 b.1111 c.1100 d.0111
2. One of the following is dual 2 to 4 decoder [ ]
a. 74X130 b.74X129 c.74LS139 d.74X119
3. _ _ _ _ _ _ contains two independent or identical 2 to 4 decoders [ ]
a. 74X139 b.74X130 c.74X129 d.74X119
4. One of the following is 3 to 8 decoder [ ]
a. 74X130 B.74X119 C.74X36 d.74X138
5. 74 X 138 has [ ]
a. three enable inputs b.two enable inputs c.four enable inputs d.one enable input
6. 10011 input in seven segment decodes as _ _ _ _ _ _ _ _ _ output. [ ]
a. 1111101 b.1011001 c.1111001 d.1111000
7. A seven segment decoder has _ _ _ _ _ _ _ _ as its input code [ ]
a. 4 bit BCD b.6 bit excess 3 c.3 bit octal d.3 bit hex
8. _ _ _ _ _ _ _ _ is seven segment decoder [ ]
a. 74X138 b.74X491 c.74X149 d.74X49
9. Blanking input in 74X49 is [ ]
a. Bi _ H b.B _ L c.Bi _ U d.Bi _ L
10. 10111 input gives _ _ _ _ _ _ _ _ _ _ _ _ output in seven segment decoder [ ]
a. 1110000 b.1110001 c.1110010 d.1100000
11. 001111111 input produce _ _ _ _ _ _ _ _ in 74 X 148, 8 bit priority encoder. [ ]
a. 11101 b.11001 c.10101 d.11100
12. XX011111 gives _ _ _ _ _ _ _ _ output in priority encoder [ ]
a. 10101 b.00101 c.10001 d.10100

13. A.Flip-Flop has 2 o/ps which are [ ]

a. always 0 B.always 1 C.always complementary D.all the above

14. A flip-flop can be made using [ ]

A.basic gates such as AND,OR,NOT BNOR gates C.NAND gates D.any of the above

15. Which of the following flip-flop is used as Latch [ ]

A.J-K flip-flop B.S-R flip-flop C.T-flip-flop D. D-flip-flop

16. A flip-flop can store ___data [ ]

A. one-bit B.2 bit C.3 bit D.4-bit

17. when an inverter place b/w the i/ps of S-R FF the resulting Flip-Flop is [ ]

A.J-K FF B.Master-slave FF C.T-FF D.D-FF

18. which of the following input combinations is not allowed in an S-R FF [ ]

A.S=0,R=0 B.S=0,R=1 C.S=1,R=0 D.S=1,R=1

19. when a flip-flop is set its output will be [ ]

A.Q=0 ,Qbar=0 B.,Q=1,Qbar=0 C.Q=0,Qbar=1 D.Q=1,Qbar=1

20. when a flip-flop is set its output will be [ ]

A.Q=0 ,Qbar=0 B.,Q=1,Qbar=0 C.Q=0,Qbar=1 D.Q=1,Qbar=1

21. Flip-Flops can be used to make [ ]

A.latches B.bounce elimination switches C.registers D.all

22. A universal register [ ]

A.accepts serial i/p B.accepts parallel i/p C.gives serial and parallel o/ps D.all above

23. The transparent latch is [ ]

A.S-R flip-flop B.D-fliup-flop C.T-flip-flop D.J-K flip-flop

24. A shift register using flip-flop is called a [ ]

A.Dynamic shift reg B.flip-flop reg C.static shift reg D.buffer shift reg

25. In sequential circuits the present input depends on [ ]

A.past i/ps only B.present i/ps only C.present as well as past i/ps D.past o/ps

26. A_____ is basic memory element [ ]

A.Flip-Flop B.Register C.Counter D.Encoder

27. A Flip-Flop has _____stable states [ ]

A.2 B.5 C.3 D.1

28. Edge triggering is also called as_____triggering [ ]
A.Dynamic B.ststic C.Low D.High

29. For a J-k Flip-flop j=1,k=1 is the _____Mode [ ]

A.Stable B.Toggle C.Delay D.Equal

30. The clocked D-latch is called _____D latch [ ]

A.Clocked B.Transperant C.Not transperant D.Normal

31. The Register which contains both shifts and parallel load capabilities___reg [ ]
A.Shift reg B.Bi-direectional Shift reg C.Universal D.SISO

32. a coded device which implements n:2^n function is called [ ]
A. encoder B. decoder C. neither A nor B D. either A or B

33. In a circuit 1x2^n functional IC, 'n' represents [ ]
A. inputs B. outputs C. select lines D. all of the above

34. functional blocks in IC HCF4543B are [ ]
A. latch B. decoder C. display driver D. all of the above

35. encoder circuit is of the form [ ]
A. n:2^n B. 2^n :n C.n:m D. m:2^n

36. priority encoder output for the combination of 'X 1 0 0" ,where 'X' represents don't care
A. 0 1 0 B. 0 1 1 C. 0 1 0 D. 1 1 1 [ ]

37. 4 Input parity checker consists of how many EX-OR gates
A. 3 B. 4 c. 5 D. 6 [ ]

38. An IC 7485 is how many bit comparator
A. 2 B. 4 C. 8 D. 16 [ ]

39. when both S=R=1 then SR flip flop output is equals to [ ]
A. 1 B. 0 C. X D. indeterminate

40. race around condition occurs In _____flip flop [ ]
A. JK B. D C. SR D. T

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