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SAMPLE COPIES OF ACTIVITIES FOR

ADVANCED AND SLOW LEARNERS

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PRINCIPAL PRINCIPAL Siddharth Institute of Engnineering & Technology Siddharth Nagar PUTTUR - 517583, Chittoor Disr.



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LPARTIVIENT OF ELECTRONICS AND COMIVIUNICATION ENGINEERIN

Academic Year: 2019-2020 Year &SEM: IV YEAR II-SEM

MICROPROCESSORS & MICROCONTROLLERS (16EC423) TUTORIAL TOPICS FOR ADVANCED LEARNERS

1. INTERFACING 7 SEGMENT DISPLAY

segment LED display is a very popular and it can display digits from 0 to 9 and quite a few characters like A, b, C, , H, E, e, F,, etc. Knowledge about how to interface a seven-segment display to a micro controller is very essential in designing embedded systems. A seven-segment display consists of seven LEDs arranged in the form of a squarish '8' slightly inclined to the right and a single LED as the dot character. Different characters can be displayed by selectively glowing the required LED segments.

Seven segment displays are of two types, common cathode and common anode. In common cathode type, the cathode of all LEDs are tied together to a single terminal which is usually labeled as 'com' Â and the anode of all LEDs are left alone as individual pins labeled as a, b, c, d, e, f, g & h (or dot). In common anode type, the anode of all LEDs are tied together as a single terminal and cathodes are left alone as individual pins. The pin out scheme and picture of a typical 7 segment LED displayis shown in the image below.





In common cathode, all the cathodes of LEDs are tied together and labeled as com. and the anode are left alone. In common anode, seven segment display all the anodes are tied together and cathodes are left freely. Below figure shows the internal connections of seven segment Display.



To display the digits on 7 segment, we need to glow different logic combinations of segments. For example if you want to display the digit 3 on seven segment then you need to glow the segments a, b,



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c, d and g. The below table show you the Hex decimal values what we need to send from PORT1 toDisplay the digits from 0 to F.

	h	g	ſ	е	d	с	b	a	hex value
	0	0	1	1	1	1	1	1	3F
H	0	0	0	0	0	1	1	0	06
2	0	1	0	1	1	0	1	1	5B
E	0	1	0	0	1	1	1	1	4 F
4	0	1	1	0	0	1	1	0	66
5	0	1	1	0	1	1	0	1	6D
6	0	1	1	1	1	1	0	1	7D
П	0	0	0	0	0	1	1	1	07
8	0	1	1	1	1	1	1	1	7 F
9	0	1	1	0	1	1	1	1	6F
R	0	1	1	1	0	1	1	1	77
Ь	0	1	1	1	1	1	0	0	7C
Ε	0	0	1	1	1	0	0	1	39
Ч	0	1	0	1	1	1	1	0	5E
Ε	0	1	1	1	1	0	0	1	79
F	0	1	1	1	0	0	0	1	71





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LOOK OP	lable	
0400	3F	
0401	06	H
0402	5B	2
0403	4F	Е
0404	66	4
0405	6D	5
0406	7D	6
0407	07	
0408	7F	B
0409	6F	9
	0400 0401 0402 0403 0403 0404 0405 0406 0407 0408 0409	0400 3F 0401 06 0402 5B 0403 4F 0404 66 0405 6D 0406 7D 0407 07 0408 7F 0409 6F

MOV DPTR,#0400H MOV A,#04H MOVC A, @A+DPTR MOV P1,A

The above picture indicates that all the 7-segment display codes are stored in ROM and in the formof look-up tables. To get those codes we use Indexed addressing mode.





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****Note**: Suppose if you want to display the year 2021, then you need to interface four 7-segmentdisplays to 8051 microcontroller. Here is the program to display 2021. In exam if they ask you todisplay some other number just change the appropriate number in program, rest of the logic is same. **Program**



2. INTERFACING 4X4 MATRIX KEYPAD

Keypads are widely used input devices being used in various electronics and embedded projects. They are used to take inputs in the form of numbers and alphabets and feed the same into system for further processing. Matrix keypad consists of set of Push buttons, which are interconnected. Like in our case we are using 4X4 matrix keypad, in which there are 4 push buttons in each of four rows. And the terminals of the push buttons are connected according to diagram. In first row, one terminal of all the 4 push buttons are connected together and another terminal of 4 push buttons are representing each of 4 columns, same goes for each row. So we are getting 8 terminals to connect with amicrocontroller.





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As shown in above circuit diagram, to interface Keypad, we need to connect 8 terminals of the keypad to any port (8 pins) of the microcontroller. Like we have connected keypad terminals to Port1 of 8051. Whenever any button is pressed we need to get the location of the button, means the corresponding ROW an COLUMN no.

- The hex keypad has 8 communication lines namely R1, R2, R3, R4, C1, C2, C3 and C4. R1 to R4 represents the four rows and C1 to C4 represents the four columns.
- When a particular key is pressed the corresponding row and column to which the terminals of the key are connected gets shorted. For example if key 1 is pressed row R1 and column C1gets shorted and so on.
- The program identifies which key is pressed by a method known as column scanning. In this method a particular row is kept low (other rows are kept high) and the columns are checked for low. If a particular column is found low then that means that the key connected betweenthat column and the corresponding row (the row that is kept low) is been pressed.
- For example if a row R1 is initially kept low and column C1 is found low during scanning, that means key 1 is pressed.

Program:

MOV DPTR, #0400H ; Base Address of lookup table for Seven Segment Code MOV P2, #0FH ; Send all 1's and make P2 an input port

REPEAT: MOV P1, #00H ; Send O's on all Rows



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MOV A, P2 ; Read the Columns CJNE A, #0FH, **PRESSED** ; If key is pressed, then go to PRESSED SJMP **REPEAT** ; Else keep checking

PRESSED: ACALL DELAY ; Call a delay routine of 20ms for key de-bouncing MOV R0, #00H ; Assume Key "0" MOV P1, #0EH ; Test for Row P1.0MOV A, P2 ; Read the Columns CJNE A, #0FH, DETECT ; P1.0 Row is Identified. Now Identify the Column

> MOV R0, #04H ; Assume Key "4" MOV P1, #0DH ; Test for Row P1.1MOV A, P2 ; Read the Columns CJNE A, #0FH, **DETECT** ; P1.1 Row is Identified. Now Identify the Column

> MOV R0, #08H ; Assume Key *"8"* MOV P1, #0BH ; Test for Row P1.2MOV A, P2 ; Read the Columns CJNE A, #0FH, DETECT ; P1.2 Row is Identified. Now Identify the Column

MOV R0, #0CH ; Assume Key "8" MOV P1, #07H ; Test for Row P1.3MOV A, P2 ; Read the Columns

- DETECT: RRC A ; Test for each Column JNC FOUND ; If no carry then Key is detected as the value of RO INC RO ; Else increment RO SJMP DETECT ; Check next Column
- FOUND: MOV A, R0 ; Transfer Key value into A register MOVC A, @A+DPTR ; Read Seven Segment Code from look-up table MOV P0, A ; Display the Key–Pressed on port 0

ACALL DELAY; Call a delay routine of 20 ms for key release

SJMP REPEAT



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SAMPLES OF NPTEL CERTIFICATES





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IT Roorkee



(12 week course)



IIT Roorkee

Indian Institute of Technology Roorkee



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This certificate is awarded to

S VENKATA SAI NAVEEN

for passing the course

Manufacturing Process Technology I & II

with Score* 99 %

Prof. Rajesh M.Hegde Chairman, Centre for Continuing Education IIT Kanpur

Jan-Apr 2020 (12 week course)

Covid-19 impacted

January 2020

semester

Prof. Satyaki Roy NPTEL Coordinator IIT Kanpur



Indian Institute of Technology Kanpur

*Continuous online assessment score

To validate and check scores: https://nptel.ac.in/noc



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R	NPT	EL	Elite Online d by the Ministry of HRD	Cer	tification ^{Idia)}	n	
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C	Inline Assignments	24.75/25	Programming Exam	25/25	Proctored Exam	25/50	
Devenu Prof. De Centre for Con	Total dra Galibal wendra Jalihal Chairman thinuing Education, IITM	number of o	andidates certified in Jul-Oct 2019 (12 week course)	this cours	e: 8505 Ti Prof.	Andrew Thangaraj	1
Roll No: NPTE	In Institute of Technology M	ladras		To	validate and check score	s: https://nptel.ac.ii	n/hoc



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PROJECT COMPLETION CERTIFICATE





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To Whomsoever It May Concern

This is to certify that **Ms. M. RUCHITHA (Reg. No:- 16F61A04H4)**, B.Tech (ECE) Third year student of the Siddharth Institute of Engineering and Technology, Puttur was placed with us for Project work from <u>30.05.19</u> to <u>29.06.19</u>.. This Project work has been organized as part of her study curriculum.

During the period, she had done a Project work with the title of "Study on Battery Charger Process" at AMARARAJA BATTERIES. Ltd. under the guidance of Mr. K. Bhanu Moorthy, Engineer, Amara Raja Batteries Ltd, Tirupathi.

M. Ruchitha has shown her keen interest while doing the Project work. We found her enthusiastic, diligent and creative. We wish her a bright future.

For Amara Raja Batteries Limited,

K. Nalini Kumar

18 Asst General Manager – Human Resources

Date: 01.07.2019

AMARA RAJA



D AMARA RAJA Johnson Control Arura Rua Hesson Controls Car Amera Reje Batteries Limited | An Amara Naja Group Company Registered Office & Works, Narakambed \$11530, Tropeti, Andria Precess, India. Tel No. 41 877 226500, Fac No. 431 877 2285400 E-mail: amerarajeBamararaje.co.in, Corporate Operations Office: TEMINAL A

Corporate generations when TenHinal, A. 1-18/1/AMR/NR, Nasakramguda, Gachibowil, Hydersbad-S00033, India 1-18/1/AMR/NR, Nasakramguda, Gachibowil, Hydersbad-S00033, India 1-18/10, 471 a0 23131000, Fax Ne. +91 40 23139901, E-mail: mstg8amararaja.co.in Weiselre, www.entersreae.co.in, Corporate Identification Number, L31402AP1985PL.0005305



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SAMPLE CERTIFICATES OF PARTICIPATIONS

DEPARTMENT OF COMPUT SRI PADMAVATI MAHILA VISV (WOMEN'S UNIVER NATIONAL LEVEL T	TER SCIENCE /AVIDYALAYAM SITY) ECHFEST
ASPIRE 2017	
21st-22nd Septembe	er
CERTIFICATE	
This is to certify that Mr./Ms. D. Harin	ath Reddy (B. Tech, FFF. W. Word)
studying in Siddartha Institute of	Engineering & Technology, Puttur
has participated in workshop on -	J
/ presented a paper entitled Identification of	Transformer Failure in
Agricultural Areas By Internet	of Things
and won the First place / Second place/ Third p	lace in Poster Presentation
Competition / Attended ASPIRE 2017.	
M.Ushaean/	\$
Prof. M. Usha Rani Co-Convener	Prof. P. Venkata Krishna Convener



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SRI VEN	KATESWARA COLLEGE OF ENGINEERING Ngineering College For Women
A DE COLOR	Karakambadi Road, TIRUPATI - 517 507, A.P.
SVCE FIRUPATI	TECH BLOOM-2016
	Certificate of Competence
This is to c	ertify that Mr/Ms. D. Having-th Redity of Siddhartha College
participated in	Paper presentation - Mathematics on 23rd April, 2016 organized by ,
Department of	GEBHS, SV Colleges, Tirupati. He/She has been awarded <u>First</u> prize.
	Northaddy
	PRINCIPAL





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This is to certify that **TAYEE NALINI**

bearing number. APSSDC/Siemens/M/45210 has successfully

completed Electrical (Home)- Expert Course

Conducted at

Siddharth Institute Of Engineering And Technology, Puttur

from 05-Mar-19 to 16-Mar-19

Siemens Industry Software Pvt. Ltd APSSDC DesignTech Systems Limited

This is an auto generated Certificate and does not require Signatures



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Cartificate of Participation	
Cerunicale of Participation	
Ars. B T Vasantha	Kumar
ha Institute of Engineering and Techn	ology
Scilab 2017 - 18	
to 03-02-2018	
	Certificate of Participation Irs. B T Vasantha ha Institute of Engineering and Technol Scilab 2017 - 18 to 03-02-2018



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NATIONAL SERVICE SCHEME CHITTOOR DISTRICT LEVEL NSS YOUTH FESTIVAL - 2018 CERTIFICATE OF PARTICIPATION Certified that Mr./Ms. T. HEMALATHA S/0, D/0 T. SURYANARAYANA studying at SIETK, PUTTUR college, JNTUA University, Andhra Pradesh attended Chittoor District Level NSS Youth Festival at SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY, PUTTUR, Andhra Pradesh during 9th JANUARY, 2018. He/ She participated in PAINTINE competition. NSS PO/ Program Coordinator Freed Chairman & Principal NSS



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INTERNSHIP CERTIFICATES







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BENNETT UNIVERSITY TIMES OF INDIA GROUP	IMMER INTERN	Sr. No. SI-20-II-50
ARTIFICIAL INTE	LLIGENCE AN	D DEEP LEARNING
СЕ	RTIFICATE OF COMPI	LETION <
This is to certify that <u>U</u> ffrom <u>Siddharth Institute of</u>	thej K f Engineering and Teo	chnology
has successfully comp	oleted <u>six</u>	weeks internship.
Duration	01 st June to 10 th Jul	<u>y</u> 2020
Venue : Bennett I Wenue : Bennett I Magnetic Science Engineering	Jniversity, Great	er Noida (U.P.) India Madhushi Verma Internship Coordinator



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July 15, 2019

SUMMER INTERNSHIP COMPLETION CERTIFICATE

This is to certify that Me. Desireddi Gari Suhasini from Siddharth Group of Institutions has successfully completed Summer Training & Internship at YDI Solutions Pvt Ltd, Bangalore from 17th June 2019, till the close of business hours of 15th July 2019 on 'Applied Machine Learning using R'.

We found her to be self starter who is motivated, honest, diligent, and hard working. Her performance as a **Intern** was good.

We wish all the best in her future endeavors.

.....

Palor*

For YDI Solutions Pvt Ltd

Kandukuri Balachahdra Reddy (Chief Data Scientist/Director)

13A, 1st floor, 18th Cross, 3rd sector, HSR Layout, Bangalore - 560102 www.ydisolutions.ai



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अनुक्रमांक/Serial No.: NB/65/07/14581/28512/2019-20

प्रमाण पत्र / CERTIFICATE

यह प्रमाण-पत्र श्री/कु. **मक्किनेनी पावनी** पुत्र/पुत्री श्री एम नागमनायुट्ट को प्रदान किया जाता है, िल्होंने इस संस्थान में दिनांक 16.03.2020 से 20.03.2020 तक कृषि मशीनीकरण संबंधी पाठ्यक्रम के अंतर्गत गहन प्रशिक्षण प्राप्त किया।

This certificate is awarded to Shri/Kum Makkineni Pavani Son/Daughter of Shri M. Nagamanaidu who has undergone intensive training on Agricultural Mechanization at this Institute from 16.03.2020 to 20.03.2020

उन्हें मुख्य रूप से निम्न लिखित विषयों में प्रशिक्षण प्रदान किया गया । He/She has been imparted to 'ring mainly on the following subjects:

- स्टेशनरी आई.सी. इंजन का अध्ययन, मरम्मत एवं ओवरहालिंग । Study, Repair and Overhauling of Stationary I.C. Engine.
- सॉयल हैल्थ कार्ड के महत्व की जानकारी | Familarization with importance of Soil Health Card.

उन्होंने प्रशिक्षण सफलतापूर्वक पूरा किया। He/She has completed the course successfully



(डॉ.पी.पी.राव)/(Dt.P.P.RAO) निदेशक/DIRECTOR

दिनांक/DATE: 20.03.2020.



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TEAM BUILDING ACTIVITIES





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HACKATHON PARTICIPATION







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STUDENT ACTIVITIES



SIDDHARTH INSTITUE OF ENGINEEERING & TECHNOLOGY (Autonomous) (Approved by AICTE & Affiliated to JNTUA, Anantapuramu) (Accredited by NAAC & NBA)

ISTE STUDENTS CHAPTER (2019-20)



CIRCULAR

Date:-28-01-2020

ISTE Students Chapter of SIETK is glad to announce that the following events are planned to be conducted for ISTE student members only. All the student members are instructed to take part in each and every event and explore themselves.

Eligibility: ISTE members only

'S. No	Name of the Event	Date of Event	Remarks
1	Idea Pitching	30-01-2020	College level
2 Guest lecture - I		01-02-2020	College Level
3	Quiz	07-02-2020	College level
4 Rangoli		14-02-2020	College Level (Girls)
5	Guest Lecture - II	22-02-2020	Department level
6	Photography	07-03-2020	College level
7	Class Decoration	12-03-2020	College level

Attractive prizes for winners and runners in each event.

ISTE student members are advised to enroll their names with the department student coordinators and
participate actively in all the events.

FACULTY ADVISOR

CONVENER

CC to : 1. Principal

2. All HOD's

3. II, III & IV classrooms

- 4. All Dept. Faculty coordinators
- 5. File

6. Notice board



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SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY Siddharth Nagar, Narayanawanam Road – 517583

DEPARMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CIRCULAR

The Managing Committee of IETE Students' Forum (ISF) constituted for the Academic year 2019-2020 is as follows:

Dr. P. Ratna Kamala
 Mr. E. Kosalendra
 Mr. P. Pavan Kumar
 Ms. S. Gayathri
 Mr. A. Rajesh
 Ms. A. Priyanka
 Ms. K. Pavithra
 Ms. C. Muneeswari
 Mr. T. Trivikram
 Mr. K. Jayanth Varma

Professor & Head, ECE	Ex-officio President
Asst. Professor, ECE	Faculty Coordinator
Asst. Professor, ECE	Student Advisor
16F61A0450 IV B.Tech.	Chairman
17F61A04F8 III B.Tech.	Hony. Secretary
17F61A04F0 III B.Tech.	Member
17F61A04E1 III B.Tech.	Member
18F65A0405 III B.Tech.	Member
18F61A04O3 III B.Tech.	Member
18F61A0487 II B. Tech.	Member

Full - 29/u/19. **CO-ORDINATOR, ISF**



HI: 4D Department Of Electronics&Communication Enge Siddharth Institute Of Engg. & Narayanavaram Road, PUTTUR-\$17.583



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SAMPLE COPIES OF ACTIVITIES FOR

SLOW LEARNERS

S.NO	ACTIVITIES	PAGE NUMBER
		NUMBER
1.	REMEDIAL CLASSES CIRCULAR	28,35&41
2.	REMEDIAL CLASSES TIMETABLE	29,36&43
3.	REMEDIAL CLASSES ATTENDANCE	30,37&44
4.	SOLVED TUTORIAL PROBLEMS FOR SLOW LEARNERS	31,38&46
5.	IMPACT ANALYIS	34,40&51



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DEPARTMENT OF MASTER OF BUSINESS ADMINISTRATION

REMEDIAL CLASSES

CIRCULAR

Academic Year: 2020-2021Year & Sem: I Year I SemName of the Subject: Business Statistics for Managers

Date: 20/04/2021

Remedial classes for I MBA students (who scored below 60% of marks in Mid-I examination) are scheduled between 4:00PM to 5:30PM. Hence the following students are instructed to attend the classes without fail as per the given schedule.

LIST	OF	STUDENTS	IDENTIFIED	AS SLOWLEARNERS

S.NO.	ROLL NO.	NAME OF THE STUDENT
1.	20F61E0003	CHAITHANYA M
2.	20F61E0018	KIRAN.V
3.	20F61E0039	VAMSI KRISHNA K
4.	20F61E0043	YESWANTH K

Signature of the Faculty

HEAD Department Of Management Studies Siduharth Institute Of Engg. & Tech Narayanavaram Road, PUTTUR-512532



(AUTONOMOUS) (Approved by AICTE, New Delhi& Affiliated to JNTUA, Ananthapuramu) (Accredited by NBA for Civil, EEE, Mech., ECE & CSE Accredited by NAAC with 'A' Grade) Puttur -517583, Chittoor District, A.P. (India)

DEPARTMENT OF MASTER OF BUSINESS ADMINISTRATION REMEDIAL CLASSES TIME TABLE

CIRCULAR

Academic Year: 2020-2021

Date: 20/04/2021

Remedial classes for I MBA students are arranged from 4:00PM to 5:30 PM on the following subjects. Hence the students are instructed to attend the classes without fail as per the given schedule.

NAME OF THE SUBJECT	NAME OF THE FACULTY	DATE		DATE		DATE		SIGNATURE OF STAFF	
		Unit-1	22/04/2021	Might					
Business Statistics for Managers	S SREENIVASULU	Unit-2	30/04/2021	Night					
		Unit-3	07/05/2021	Nig					
		Unit-4	15/05/2021	Nizel					
		Unit-5	21/05/2021	nail					

HOD

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HEAD Department Of Management Studies Siddharth Institute Of Engg. & Tools Narayanavaram Road, PUTTHEREPORT



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BUSINESS STATISTICS FOR MANAGERS

ATTENDANCE SHEET

Academic Year: 2020-2021

Date: 21/05/2021

S.NO.	ROLL NO.	NAME OF THE STUDENT	DAY1	DAY2	DAY3	DAY4	DAY5
1.	20F61E0003	CHAITHANYA M	P	P	P	P	P
2.	20F61E0018	KIRAN.V	P	A	P	P	P
3.	20F61E0039	VAMSI KRISHNA K	P	P	P	P	A
4.	20F61E0043	YESWANTH K	A	P	P	P	P

TOPICS COVERED: DAY-1 1) Measures of central tendency 2) Measures of Dispersion DAY-3 1) Correlation 2) Regression DAY-5 1) t-test, Z-test 2) Chi-Square test

DAY-2

Classification of data
 Tabulation of Data
 DAY-4
 Hypothesis testing process

Signature of Faculty

HEAD Department Of Management Studies Siddharth Institute Of Engg. & Tech Narayanavaram Road, PUTNIR-612583.



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DEPARTMENT OF MASTER OF BUSINESS ADMINISTRATION

BUSINESS STATISTICS FOR MANAGERS TUTORIAL PROBLEMS FOR SLOW LEARNERS

1. MEASURES OF CENTRAL TENDENCY

Measures of Central Tendency

Measures of central tendency describe a set of data by identifying the central position in the data set as a single representative value. There are generally three measures of central tendency, commonly used in statistics- mean, median, and mode. Mean is the most common measure of central tendency used to describe a data set.

We come across new data every day. We find them in newspapers, articles, in our bank statements, mobile and electricity bills. Now the question arises whether we can figure out some important features of the data by considering only certain representatives of the data. This is possible by using measures of central tendency. In the following sections, we will look at the different measures of central tendency and the methods to calculate them.

What are Measures of Central Tendency?

Measures of central tendency are the values that describe a <u>data</u> set by identifying the central position of the data. There are 3 main measures of central tendency - <u>Mean</u>, <u>Median</u> and <u>Mode</u>.

- Mean- Sum of all observations divided by the total number of observations.
- Median- The middle or central value in an ordered set.
- Mode- The most frequently occurring value in a data set.

Measures of Central Tendency Definition

The central tendency is defined as the statistical measure that can be used to represent the entire distribution or a dataset using a single value called a measure of central tendency. Any of the measures of central tendency provides an accurate description of the entire data in the distribution.

2. MEASURES OF DISPERSION

Measures of Dispersion

The following data provide the runs scored by two batsmen in the last 10 matches.

Batsman A: 25, 20, 45, 93, 8, 14, 32, 87, 72, 4

Batsman B: 33, 50, 47, 38, 45, 40, 36, 48, 37, 26



1. Range

The difference between the largest value and the smallest value is called Range.

Range R = L - S

Coefficient of range = (L - S) / (L + S)

where L - Largest value; S - Smallest value

Example 8.1 Find the range and coefficient of range of the following data: 25, 67, 48, 53, 18, 39, 44.

Solution Largest value L = 67; Smallest value S = 18

Range R = L - S = 67 - 18 = 49

Coefficient of range = (L - S) / (L + S)

Coefficient of range = (67 - 18) / (67 + 18) = 49/85

= 0.576

Example 8.2 Find the range of the following distribution.

Age (in years)	16-18	18-20	20-22	22-24	24-26	26-28
Number of students	0	4	6	8	2	2

Solution Here Largest value L = 28Smallest value S = 18Range R = L - S



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3. CORRELATION

data by using origin & scale

- × 100 800 300 400 500 600 700
- Y 30 50 60 80 100 130

	*:	n: -x1 - 4	Y: V	- 4-B	VV	U2-	V ²
	160	300 ,	30	-50	15000	90,000	9.500
	200	.: - 2 001	50	- 30 0	6000	40,000	100 JU
	300	- 10 0-	60	- 20 .	2000	10000	1. 400 cm
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	600	800	10 *	30 .	6000	40,000	doo .
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Y(wy) = 1200- 2020 JAZUE (EU) JAZUE (EU)2

 $= \frac{3,29,000}{3,29,000} = +0.99$

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DEPARTMENT OF MASTER OF BUSINESS ADMINISTRATION

BUSINESS STATISTICS FOR MANAGERS

IMPACT ANALYSIS

Academic Year: 2020-2021

YEAR /SEM: I /I

S.NO	ROLL NO.	STUDENT NAME	MID-I MARKS (30 Marks)	MID-II MARKS (30 Marks)
1.	20F61E0003	CHAITHANYA M	10	25
2.	20F61E0018	KIRAN.V	15	24
3.	20F61E0039	VAMSI KRISHNA K	10	24
4	20F61E0043	YESWANTH K	9	22



Signature of the Faculty

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HEAD Department Of Monage St Studies Siddharth Institute Of Engg. & T Narayanayaram Road, PUTTUR-517.



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REMEDIAL CLASSES

CIRCULAR

Academic Year: 2020-2021Year & Sem: II Year I SemName of the Subject: Microprocessors & Microcontrollers (19EC0421)

Remedial classes for II B.Tech CSIT students (who scored below 60% of marks in Mid-I examination) are scheduled between 4:00PM to 5:30PM at Room no: AUDI-301. Hence the following students are instructed to attend the classes without fail as per the given schedule.

S.NO.	ROLL NO.	NAME OF THE STUDENT
1.	19F61A0609	HIMA BINDU.N
2.	19F61A0613	LAKSHMI VARAPRASAD.M
3.	19F61A0621	MUNI VAMSI.N
4.	19F61A0622	NAVEEN REDDY.D
5.	19F61A0623	NETAJI.V
6.	19F61A0630	RAHUL.B
7.	19F61A0638	SRAVANLG
8.	19F61A0646	UMAMAHESH.N

LIST OF STUDENTS IDENTIFIED AS SLOWLEARNERS

Signature of the Faculty

HOD

Date:21 /05/2021

HEAD Depl. of Computer Science & Information Technology SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY Siddharth Nagar, Narayanavanam Road, PUTTUR, Chittoor Dt. (A.P.)-517583. Ś.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY

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DEPARTMENT OF COMPUTER SCIENCE & INFORMATION TECHNOLOGY REMEDIAL CLASSES TIME TABLE

CIRCULAR

Academic Year: 2020-2021

Date: 21/05/2021

Remedial classes for II B.Tech CSIT students are arranged from 4:00PM to 5:30 PM on the following subjects at Room no: AUDI-301. Hence the students are instructed to attend the classes without fail as per the given schedule.

NAME OF THE SUBJECT	NAME OF THE FACULTY	1	DATE	SIGNATURE OF STAFF
		Unit-1	24/05/2021	
Microprocessors &		Unit-2	31/05/2021	
Microprocessors &	D.Muneendra	Unit-3	07/06/2021	de
Microcontrollers		Unit-4	14/06/2021	Tet
	1	Unit-5	21/06/2021	
		Unit-1	25/05/2021	
		Unit-2	01/06/2021	
Compiler Design	D.Viswasahithya	Unit-3	08/06/2021	Of partities
		Unit-4	15/06/2021	Drown O
Carrier Contractor		Unit-5	22/06/2021	*
		Unit-1	26/05/2021	
		Unit-2	02/06/2021	
Web Technologies	N.Poornima	Unit-3	09/06/2021	10 David
		Unit-4	16/06/2021	Nectanor
	and the second second	Unit-5	23/06/2021	

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HEAD Dept. of Computer Science & Information Technology SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY Giddharth Nagar, Narayanavanam Road. PUTTUR, Chittoor Dt. (A.P.)-517583.



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DEPARTMENT OF COMPUTER SCIENCE & INFORMATION TECHNOLOGY

MICROPROCESSORS & MICROCONTROLLERS (19EC0421)

ATTENDANCE SHEET

Academic Year: 2020-2021

Date: 24/5/2021 to 21/6/2021

S.NO.	ROLL NO.	NAME OF THE STUDENT	DAY1	DAY2	DAY3	DAY4	DAY5
1.	19F61A0609	HIMA BINDU.N	P	P	P	P	P
2.	19F61A0613	LAKSHMI VARAPRASAD.M	P	A	P	P	P
3.	19F61A0621	MUNI VAMSI.N	P.	P	P	P	P
4.	19F61A0622	NAVEEN REDDY.D	P	P	P	P	P
5.	19F61A0623	NETAJI.V	P	P	P	P.	A
6.	19F61A0630	RAHUL.B	A	A	A	P	P
7.	19F61A0638	SRAVANI.G	P	P	P	P	A
8.	19F61A0646	UMAMAHESH.N	P	P	P	P	P

TOPICS COVERED:

DAY-1

1) Microprocessor Architecture

2) Example of a microcomputer system

3) Microprocessor controlled temperature system (MCTS)

DAY-3

- 1) Counters and timers
- 2) Interrupts

3) 8051 microcontroller hardware

DAY-5

- 1) D/A and A/D Conversion -
- 2) Displays

DAY-2

- 1) The 8085 Microprocessor
- 2) Data format and Data Storage
- 3) Overview of the 8085 Instruction set

DAY-4

- 1) Logical operations
- 2) Addressing modes
- 3) Programs using Interrupts

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DEPARTMENT OF COMPUTER SCIENCE & INFORMATION TECHNOLOGY MICROPROCESSORS & MICROCONTROLLERS

TUTORIAL FOR SLOW LEARNERS

UNIT 2 i 16 bit Microprocessor Instruction Set (
and ALP	
programmer Model of Intel 5086	
3086 has 20 address lines I.e. I Mis of memory	
It is divided into 4 segments each 64 KB program mu	-
15 1 9 15 9 FATT	
ES BE Separat Pililing:	**
General pusposes 16 bit Registers Ax, BX FX, DX	
15 th 87 - 8 the	
AH AL HIS HIS HEL- keet	2
Che L CL for pfister st 251 - AFI- I	
DH DL	
operand Types	
ALL RUP, Word, DW	
+ Bytes - Shit . Higned - byte, -	0
+ herds - 16 bit Unsigned - shore, song, 1000	3
t short Integers - & bit	
+ Integers - 10 bit	
+ Long Integers - 32 bit	
* string - series of bytes (er) series of words series	
in semiential memory ascarting	10
Instruction formed	No.
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Instruction formed An Instruction length may marge between 1 to 6 by	20
Instruction formed An Instruction clength may marge between 1 to 6 by 1 mpre 1 whe Topicon Reg	20

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duction

Inchancion	
Microp	roussor based system will contain memory, Anput
writ and	output unit.
olp	derices in 7 segment LED Display
-11	CRT Monutor
z	panjinten
21p	device -> Key board, Digital inputs (m)
	Analog inputs service
Support	Ic chips for peripheral interfacing of the
411	A OF MP
8085 and	so are mit. protoheral Interface (Intel 8255)
+	programmable loupide convoller (intel 8379)
*	Keyboard and Display and (Entel 8253/825
*	programmable interval times critic of 1
others Dr Ind	A conpoller terrupt conpoller.
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General	is and outputs the data through
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6 1 1 1	we port .

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DEPARTMENT OF COMPUTER SCIENCE & INFORMATION TECHNOLOGY

MICROPROCESSORS & MICROCONTROLLERS

IMPACT ANALYSIS

Academic Year: 2020-2021

Year /Sem: II /I

S.NO	ROLL NO.	STUDENT NAME	MID-I MARKS (30 Marks)	MID-II MARKS (30 Marks)
1.	19F61A0609	HIMA BINDU.N	17	19
2.	19F61A0613	LAKSHMI VARAPRASAD.M	15	19
3.	19F61A0622	NAVEEN REDDY.D	06	19
4.	19F61A0623	NETAJI.V	10	23
5.	19F61A0630	RAHUL.B	10	20
6.	19F61A0638	SRAVANI.G	17	21
7.	19F61A0646	UMAMAHESH.N	15	18



Signature of the Faculty



HEAD Depl. of Computer Science & Information Technology SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLogi Siddharth Nagar, Narayanayanam Road; PUTTUR, Chittoor DI. (A.P.3-5175d3;



SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY (AUTONOMOUS) (Approved by AICTE, New Delhi& Affiliated to JNTUA, Ananthapuramu) (Accredited by NBA for Civil, EEE, Mech., ECE & CSE Accredited by NAAC with 'A' Grade) Puttur -517583, Chittoor District, A.P. (India) DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

REMEDIAL CLASSES

CIRCULAR

Date: 21/10/2016

Academic Year: 2016-2017Year & Sem: IV YEAR I-SEMName of the Subject: Embedded Systems (13A04709)

Remedial classes for IV-B.Tech ECE students (who scored below 60% of marks in Mid-I examination) are scheduled between 4:00PM to 5:30PM at B-202. Hence, the following students are instructed to attend the classes without fail as per the given schedule.

S.NO.	ROLL NO.	NAME OF THE STUDENT			
1.	13F61A0454	GURUPRAKASH.P			
2.	13F61A0480	JOSHUA.J			
3.	13F61A0483	JYOTHI.M			
4.	13F61A0490	KAVYASREE.V			
5.	13F61A04A9	MADHURI R			
6.	13F61A04B5	MANASA.A			
7.	13F61A04D6	PAVAN KUMAR.M			
8.	14F65A0402	ANANDHAN.G			
9.	14F65A0421	PURUSHOTHAM.N			
10.	14F65A0422	RAGHUVARAN.G			
11.	14F65A0425	SARATH BABU.G			
12.	14F65A0427	THAMILARASAN.N			
13.	14F65A0428	THAYAGARAJAN.M			

LIST OF STUDENTS IDENTIFIED AS SLOWLEARNERS



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	rutui -317383, Cilitto	or District, A.F. (India)
14.	14F65A0432	VIJAY KUMAR.C
15.	12F61A04C7	OMKIRAN.P
16.	12F61A04C9 P.PADMALATHA	
17.	12F61A04D3	R PAVAN KUMAR
the second s		

Signature of the Faculty

HEAD Dept. of Electronics & Communication Engg Biddharth Institute of Engg. & Tech Narayanavanam Road, Puttur-517 583.



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

REMEDIAL CLASSES TIME TABLE

CIRCULAR

Academic Year: 2016-2017

Date: 21/10/2016

Remedial classes for IVB.Tech ECE students are arranged from 04:00PM to 05:30 PM on the following subjects at B-203. Hence the students are instructed to attend the classes without fail as per the given schedule.

NAME OF THE SUBJECT	NAME OF THE FACULTY	DATE		SIGNATURE OF STAFF
		Unit-1	24/10/2016	
Embedded Systems	P.Pavan Kumar	Unit-2	31/10/2016	00
		Unit-3	07/11/2016	10
		Unit-4	14/11/2016	/
		Unit-5	21/11/2016	
	K.S.Deveswari	Unit-1	25/10/2016	~
Digital Imaga		Unit-2	01/11/2016	4-
processing		Unit-3	08/11/2016	A
		Unit-4	15/11/2016	-0
		Unit-5	22/11/2016	
Optical Fibre Communication	P.Vijaya	Unit-1	26/10/2016	
		Unit-2	02/11/2016	0 /.
		Unit-3	09/11/2016	Nilay
		Unit-4	16/11/2016	1.120
		Unit-5	23/11/2016	
Wireless Communication	T.V.A.BhanuPrakash	Unit-1	27/10/2016	
		Unit-2	03/11/2016	Kaob
		Unit-3	10/11/2016	TBhanyour.
		Unit-4	17/11/2016	1.10
		Unit-5	24/11/2016	

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EMBEDDED SYSTEMS (13A04709)

ATTENDANCE SHEET

Academic Year: 2016-2017

Date: 24/10/2016 to 21/11/2016

S.NO	ROLL NO.	STUDENT NAME	DAY1	DAY2	DAY3	DAY4	DAY5
1.	13F61A0454	GURUPRAKASH.P	P	P	P	P	P
2.	13F61A0480	JOSHUA.J	P	P	P	P	P
3.	13F61A0483	JYOTHI.M	P	P	P	P	P
4.	13F61A0490	KAVYASREE.V	P	P	P	P	P
5.	13F61A04A9	MADHURI R	P	P	D	P	P
6.	13F61A04B5	MANASA.A	P	P	P	P	P
7.	13F61A04D6	PAVAN KUMAR.M	P	P	P	P	P
8.	14F65A0402	ANANDHAN.G	P	P	P	P	P
9.	14F65A0421	PURUSHOTHAM.N	P	P	P	D	P
10.	14F65A0422	RAGHUVARAN.G	8	P	P	P	P
11.	14F65A0425	SARATH BABU.G	8	P	P	P	P
12.	14F65A0427	THAMILARASAN.N	P	P	P	P	P
13.	14F65A0428	THAYAGARAJAN.M	P	P	P	D	P
14.	14F65A0432	VIJAY KUMAR.C	P	P	P	P	P
15.	12F61A04C7	OMKIRAN.P	P	A	P	A	P
16.	12F61A04C9	P.PADMALATHA	P	P	P	P	P
17.	12F61A04D3	R PAVAN KUMAR	P	P	P	A	P

TOPICS COVERED:

DAY-1

1) Embedded system overview, applications, features

2)CISC Vs RISC design philosophy, Von-Neumann Vs Harvard architecture

3) Instruction set and instruction formats

4) Weighing Machine application using MSP430



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DAY-2

- 1)on-chip peripherals (analog and digital)
- 2) Low Power aspects of MSP430
- 3) Interrupt programming.
- 4) Watchdog timer.

DAY-3

- 1) Timer & Real Time Clock (RTC)
- 2) Timing generation and measurements
- 3) Analog interfacing and data acquisition
- 4)Remote Controller of Air Conditioner Using MSP430

DAY-4

1)Serial communication basics

2) Synchronous/Asynchronous interfaces (like UART, USB, SPI, and I2C).

3)Implementing and programming UART, I2C, SPI

4) A Low-Power Battery less Wireless Temperature & Humidity Sensor with Passive Low Frequency RFID

DAY-5

- 1) IoT overview and architecture
- 2) Embedded Wi-Fi
- 3) Building IoT applications using CC3100 user API for connecting sensors.

4)Implementing Wi-Fi Connectivity in a Smart Electric Meter

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EMBEDDED SYSTEMS (13A04709)

TOPICS REVISED FOR SLOW LEARNERS

Architecture of Embedded system:



Central Processing Unit:

The CPU in the embedded system may be a general purpose processor like a microcontroller or a special purpose processor like a DSP (Digital signal processor). But any CPU consists of of an Arithmetic Logic Unit (ALU), a Control Unit (CU), and many internal registers that are connected by buses. The ALU performs all the mathematical operations (Add, Sub, Mul, Div), logical operations (AND, OR), and shifting operations within CPU

Memory:

Embedded system memory can be either on-chip or off-chip. The memory is divided into Data Memory and Code Memory. Most of data is stored in Random Access Memory (RAM) and code is stored in Read Only Memory (ROM).

Communication Interfaces:

To transfer the data or to interact with other devices, the embedded devices are provided the various communication interfaces like RS232, RS422, RS485, USB, SPI(Serial Peripheral Interface), SCI (Serial Communication Interface), Ethernet etc.



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Application Specific Circuitry:

The embedded system sometimes receives the input from a sensor or actuator. In such situations certain signal conditioning circuitry is needed. This hardware circuitry may contain ADC, Op-amps, DAC etc. Such circuitry will interact with the embedded system to give correct output.

Address bus and data bus:

System bus is a single bus that helps all major components of a computer to communicate with each other. It is made up of an address bus, data bus and a control bus. The data bus carries the data to be stored, while address bus carries the location to where it should be stored.

Clock:

The clock is used to control the clocking requirement of the CPU for executing instructions and the configuration of timers.



Overview of MSP430

The MSP430 is a 16-bit microcontroller that has a number of special featuresnot commonly available with other microcontrollers:

- Complete system on-a-chip includes LCD control, ADC, I/O ports,
- ROM, RAM, basic timer, watchdog timer, UART, etc.
- Extremely low power consumption only 4.2 nW per instruction, typical
- High speed 300 ns per instruction @ 3.3 MHz clock, in register and register addressing mode
- RISC structure 27 core instructions



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- Orthogonal architecture (any instruction with any addressing mode)
- Seven addressing modes for the source operand
- · Four addressing modes for the destination operand
- Constant generator for the most often used constants (-1, 0, 1, 2, 4, 8)
- Only one external crystal required a frequency locked loop (FLL) oscillator derives all internal clocks
- Full real-time capability stable, nominal system clock frequency is available after only six clocks when the MSP430 is restored from low-power mode (LPM) 3; no waiting for the main crystal to begin oscillation and stabilize
- The 27 core instructions combined with these special features make it easy to program the MSP430 in assembler or in C, and provide exceptional flexibility and functionality. For example, even with a relatively low instruction count of 27

3. Write a program to transfer the data by using following serial interfaces in MSP430

(i) SPI (ii) UART

Answer:

(i) Programming SPI using USCI module in MSP430

The recommended USCI initialization/re-configuration process is:

□ Set UCSWRST (BIS.B #UCSWRST, &UCxCTL1);

- \Box Initialize all USCI registers with UCSWRST = 1 (including UCxCTL1);
- □ Configure ports;
- □ Clear UCSWRST via software (BIC.B #UCSWRST, &UCxCTL1);
- □ Enable interrupts (optional) via UCxRXIE and/or UCxTXIE

#include <msp430.h>
volatile char received_character = 0;
int main(void) {
WDTCTL = WDTPW + WDTHOLD; // Stop WDT
P1DIR |= BIT5; // for selecting of slave device(STE/SS)
P1OUT |= BIT5; // Set STE bit to high
P1SEL = BIT1 | BIT2 | BIT4; // Select 1-SOMI(RXB),2-SIMO(TXB),4-SCLK
P1SEL2 = BIT1 | BIT2 | BIT4; // Select 1-SOMI(RXB),2-SIMO(TXB),4-SCLK
UCA0CTL1 = UCSWRST //Configure Software reset
UCA0CTL0 |= UCCKPH + UCMSB + UCMST + UCSYNC;//3-pin,8-bit SPI MST



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UCA0CTL1 |= UCSSEL_2; // SMCLK UCA0BR0 |= 0x02; // divide by 2 UCA0BR1 = 0; // divide by 1 UCA0MCTL = 0; // No modulation UCA0CTL1 &= ~UCSWRST; // **Initialize USCI state machine** P1OUT &= (~BIT5); // make STE low to Select Device while (!(IFG2 & UCA0TXIFG)); // USCI_A0 TX buffer ready? UCA0TXBUF = 0xAA; // Send 0xAA over SPI to Slave while (!(IFG2 & UCA0RXIFG)); // USCI_A0 RX Received? received_character = UCA0RXBUF; // Store received data P1OUT |= (BIT5); // Unselect Device }

(ii) Programming UART using USCI module in MSP430

#include <msp430.h>

int main(void) {

WDTCTL = WDTPW + WDTHOLD; // Stop WDT

DCOCTL = 0; /* Use Calibration values for 1MHz Clock DCO*/

BCSCTL1 = CALBC1 1MHZ;

DCOCTL = CALDCO_1MHZ;

P1SEL = BIT1 | BIT2 ; /* Configure Pin Muxing P1.1 RXD and P1.2 TXD */

P1SEL2 = BIT1 | BIT2;

UCA0CTL1 = UCSWRST; /* Place UCA0 in Reset to be configured */

/* Configure */

UCA0CTL1 |= UCSSEL_2; // SMCLK

UCA0BR0 = 104; // 1MHz 9600

UCA0BR1 = 0; // 1MHz 9600

UCA0MCTL = UCBRS0; // Modulation UCBRSx = 1

UCA0CTL1 &= ~UCSWRST; /* Take UCA0 out of reset */

IE2 |= UCA0RXIE; /* Enable USCI_A0 RX interrupt */

__bis_SR_register(LPM0_bits + GIE); // Enter LPM0, interrupts enabled

}

/* Echo back RXed character, confirm TX buffer is ready first */

#pragma vector=USCIAB0RX_VECTOR

__interrupt void USCI0RX_ISR(void)



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while (!(IFG2&UCA0TXIFG)); // USCI_A0 TX buffer ready? UCA0TXBUF = UCA0RXBUF; // TX -> RXed character
}

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING EMBEDDED SYSTEMS (13A04709)

IMPACT ANALYSIS

Academic Year: 2016-2017

YEAR /SEM: IV /I

S.NO	ROLL NO.	STUDENT NAME	MID-I MARKS (30 Marks)	MID-II MARKS (30 Marks)
1.	13F61A0454	GURUPRAKASH.P	16	20
2.	13F61A0480	JOSHUA.J	13	23
3.	13F61A0483	JYOTHI.M	15	25
4.	13F61A0490	KAVYASREE.V	16	26
5.	13F61A04A9	MADHURI R	13	25
б.	13F61A04B5	MANASA.A	16	23
7.	13F61A04D6	PAVAN KUMAR.M	17	20
8.	14F65A0402	ANANDHAN.G	16	24
9.	14F65A0421	PURUSHOTHAM.N	16	23
10.	14F65A0422	RAGHUVARAN.G	17	25
11.	14F65A0425	SARATH BABU.G	16	23
12.	14F65A0427	THAMILARASAN.N	11	20
13.	14F65A0428	THAYAGARAJAN.M	14	24
14.	14F65A0432	VIJAY KUMAR.C	15	23
15.	12F61A04C7	OMKIRAN.P	8	15
16.	12F61A04C9	P.PADMALATHA	14	21
17.	12F61A04D3	R PAVAN KUMAR	8	20



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