M. Tech. (Electronics & Communication Engineering)
Specialization: VLSI

I M.Tech -I Sem

S. No	Course Code	Course Name	L	T	P	Credits
1	18EC4201	VLSI Technology	3	0	-	3
2	18EC4202	Digital IC Design	3	0	-	3
Program Elective -I						
3	18EC4203	ASIC Design	3	0	-	3
	18EC4204	System Modeling & Simulation				
	18EC4101	Embedded System Design				
Program Elective -II						
4	18EC4205	Verilog HDL	3	0	-	3
	18EC4206	Analog IC Design				
	18EC4015	Image & Video Processing				
5	18EC4207	Digital Electronic Circuits Lab (Virtual Lab)	-	-	4	2
6	18EC4208	Digital IC Design Lab	-	-	4	2
7	18HS0823	Research Methodology and IPR	2	0	-	2
Audit Course-I						
8	18HS0818	English for Research Paper Writing	2	0	-	0
	18CE1029	Disaster Management				
	18HS0825	Sanskrit for Technical Knowledge				
	18HS0826	Value Education				
Contact Periods/ Week			16	-	8	**18**
			Total/ Week:24			

I M.Tech -II Sem

S. No	Course Code	Course Name	L	T	P	Credits
1	18EC4209	FPGA Architectures & Applications	3	0	-	3
2	18EC4210	Low Power VLSI Design	3	0	-	3
Program Elective -III						
3	18EC4211	Nano Electronics	3	0	-	3
	18EC4212	Algorithms for VLSI Design Automation				
	18EC4001	Advanced Digital System Design				
Program Elective -IV						
4	18EC4213	Testing & Testability	3	0	-	3
	18EC4104	Real Time Operating System				
	18EC4214	Solid State Device Modeling and Simulation				
5	18EC4215	Mixed Signal Lab	-	-	4	2
6	18EC4216	Digital VLSI Design Lab (Virtual Lab)	-	-	4	2
7	18EC4217	Mini Project	-	-	4	2

Audit Course -II						
8	18HS0829	Constitution of India	2	0	-	0
	18HS0827	Pedagogy Studies				
	18HS0828	Stress Management by Yoga				
	18HS0819	Personality Development Through Life Enlightenment Skills.				
Contact Periods/ Week			14	-	12	**18**
			Total/ Week:26			

II M.Tech -I Sem

S. No	Course Code	Course Name	L	T	P	Credits
Program Elective V						
1	18EC4218	Scripting Language for VLSI Design Automation	3	0	-	3
	18EC4219	Nano Materials and Nanotechnology				
	18EC4008	Wireless Sensor Networks				
Open Elective						
2	18HS0824	Business Analytics	3	0	-	3
	18ME3121	Industrial Safety				
	18ME3122	Advanced Operations Research				
	18CE1028	Cost Management of Engineering Projects				
	18ME3123	Composite Materials				
	18EE2128	Waste to Energy				
3	18EC4220	Dissertation Phase I	--	--	20	10
Contact Periods/ Week			6	-	20	**16**
			Total/ Week:26			

II M.Tech -II Sem

S. No	Course Code	Course Name	L	T	P	Credits
1	18EC4221	Dissertation Phase II	--	--	32	16
			Total/ Week:32			

List of Subjects

S No.	Subject Code	Subject Name
1.	18EC4201	VLSI Technology
2.	18EC4202	Digital IC Design
3.	18EC4203	ASIC Design
4.	18EC4204	System Modeling & Simulation
5.	18EC4101	Embedded System Design
6.	18EC4205	Verilog HDL
7.	18EC4206	Analog IC Design
8.	18EC4015	Image & Video Processing
9.	18EC4207	Digital Electronic Circuits Lab (Virtual Lab)
10.	18EC4208	Digital IC Design Lab
11.	18HS0823	Research Methodology and IPR
12.	18HS0818	English for Research Paper Writing
13.	18CE1029	Disaster Management
14.	18HS0825	Sanskrit for Technical Knowledge
15.	18HS0826	Value Education
16.	18EC4209	FPGA Architectures & Applications
17.	18EC4210	Low Power VLSI Design
18.	18EC4211	Nano Electronics
19.	18EC4212	Algorithms for VLSI Design Automation
20.	18EC4001	Advanced Digital System Design
21.	18EC4213	Testing & Testability
22.	18EC4104	Real Time Operating Systems
23.	18EC4214	Solid State Device Modeling and Simulation
24.	18EC4215	Mixed Signal Lab
25.	18EC4216	Digital VLSI Design Lab (Virtual Lab)
26.	18EC4217	Mini Project
27.	18HS0829	Constitution of India
28.	18HS0827	Pedagogy Studies
29.	18HS0828	Stress Management by Yoga
30.	18HS0819	Personality Development Through Life Enlightenment Skills.
31.	18EC4218	Scripting Language for VLSI Design Automation
32.	18EC4219	Nano Materials and Nanotechnology
33.	18EC4008	Wireless Sensor Networks
34.	18HS0824	Business Analytics
35.	18ME3121	Industrial Safety
36.	18ME3122	Advanced Operations Research
37.	18CE1028	Cost Management of Engineering Projects
38.	18ME3123	Composite Materials
39.	18EE2128	Waste to Energy
40.	18EC4220	Dissertation Phase I
41.	18EC4221	Dissertation Phase II

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4201) VLSI TECHNOLOGY
(Common to VLSI & ES)

I M. Tech -I Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
	3	**-**	**3**

UNIT I

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi-CMOS) Technology Trends and Projections.

BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BiCMOS CIRCUITS: I_{ds} - V_{ds} Relationships, Threshold Voltage V_t, gm, g_{ds} and ω_o, Pass Transistor, MOS, CMOS & Bi-CMOS Inverters, $Z_{p.u}/Z_{p.d}$, MOS Transistor Circuit Model, Latch-Up in CMOS Circuits.

UNIT II

LAYOUT DESIGN AND TOOLS: Transistor Structures, wires and vias, Scalable Design Rules, Layout Design Tools.

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT III

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT IV

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, High Level Synthesis, Architecture for Low Power, SOCs and Embedded CPUs, Architecture Testing.

UNIT V

INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN: Layout Synthesis and Analysis, Scheduling and Printing, Hardware-Software Co-design, Chip Design Methodologies- A Simple Design Example.

TEXT BOOKS:

1. *Essentials of VLSI Circuits and Systems*, K. Eshraghian et.al (3 authors) PHI of India Ltd.,2005.
2. *Modern VLSI Design*, 3rd Edition, Wayne Wolf, Pearson Education, fifth Indian Reprint, 2005.

REFERENCES:

1. *Principals of CMOS Design*, N.H. E Weste, K. Eshraghian, Adison Wesley, 2nd Edition.
2. *Introduction to VLSI Design*, Fabricius, MGH International Edition, 1990.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4202) DIGITAL IC DESIGN
(Common to VLSI & ES)

I M. Tech -I Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT I

CMOS Inverters -Static and Dynamic Characteristics, Static and Dynamic CMOS Design-Domino and NORA Logic - Combinational and Sequential Circuits.

UNIT II

Method of Logical Effort for Transistor Sizing -Power Consumption in CMOS gates- Low Power CMOS Design, Arithmetic Circuits in CMOS VLSI - Adders- Multipliers- Shifter - CMOS Memory Design - SRAM and DRAM

UNIT III

Bipolar Gate Design- BiCMOS Logic - Static and Dynamic Behavior -Delay and Power Consumption in BiCMOS Logic.

UNIT IV

LAYOUT DESIGN RULES: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load**.**

UNIT V

SUBSYSTEM DESIGN PROCESS: General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU Sub-System, Implementing ALU Functions with an Adder, Carry-look-ahead Adders, Multipliers, Serial Parallel Multipliers, Pipeline Multiplier Array, Modified Booth's Algorithm.

TEXT BOOKS:

1. *CMOS Digital Integrated Circuits - Analysis & Design*-Sung-Mo Kang & Yusuf Leblebici, MGH, Second Ed., 1999.
2. *Digital Integrated Circuits - A Design Perspective*, Jan M Rabaey, Prentice Hall, 1997.
3. *Introduction to VLSI Design*, Eugene D Fabricus, McGraw Hill International Edition.1990.

REFERENCES:

1. *Digital Integrated Circuit Design,* Ken Martin, Oxford University Press, 2000.
2. *Principles of CMOS VLSI Design - A System Perspective,* Neil H E West and Kamran Eshranghian, Addision-Wesley 2nd Edition,2002.
3. *CMOS circuit design, layout, and simulation,* R. J. Baker, H. W. Li, and D. E. Boyce, New York: IEEE Press, 1998.
4. *Analysis and Design of Digital Integrated Circuits*, David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Third Edition, McGraw-Hill, 2004.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4203) ASIC DESIGN
(Program Elective -I)

I M. Tech -I Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT I

ASIC DESIGN STYLES: Introduction – Categories-Gate Arrays-Standard Cells-Cell Based Asics-Mixed Mode and Analogue ASICs – PLDs.

ASICS – PROGRAMMABLE LOGIC DEVICES: Overview – PAL –Based PLDs: Structures, PAL Characteristics – FPGAs: Introduction, Selected Families – Design Outline.

UNIT II

ASICS –DESIGN ISSUES: Design Methodologies and Design Tools – Design for Testability – Economies.

ASIC CHARACTERISTICS AND PERFORMANCE: Design Styles, Gate Arrays, Standard Cell -Based Asics, Mixed Mode and Analogue Asics.

UNIT III

ASICS-DESIGN TECHNIQUES: Overview- Design Flow and Methodology-Hardware Description Languages-Simulation and Checking-Commercial Design Tools- FPGA Design Tools: XILINX, ALTERA.

UNIT IV

LOGIC SYNTHESIS, SIMULATION AND TESTING: Verilog and Logic Synthesis - VHDL and Logic Synthesis - Types of Simulation -Boundary Scan Test - Fault Simulation-Automatic Test Pattern Generation.

UNIT V

ASIC CONSTRUCTION: Floor Planning, Placement and Routing System Partition.

FPGA PARTITIONING: Partitioning Methods-Floor Planning- Placement-Physical Design Flow-Global Routing-Detailed Routing –Special Routing-Circuit Extraction-DRC.

TEXT BOOKS:

1. *Integrated circuit engineering*, L.J.Herbst, OXFORD SCIENCE Publications, 1996.

REFERENCES:

1. *Application -Specific integrated circuits*, M.J.S.Smith, Addison-Wesley Longman Inc 1997.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4204) SYSTEM MODELLING & SIMULATION
(Program Elective -I)

I M. Tech -I Sem. (E.C.E) (VLSI)

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UNIT I

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single Server Queuing System, Simulation of Inventory System, Alternative Approach to Modeling and Simulation.

SIMULATION SOFTWARE: Comparison of Simulation Packages with Programming Languages, Classification of Software, Desirable Software Features, General Purpose Simulation Packages – Arena, Extend and Others, Object Oriented Simulation, Examples of Application Oriented Simulation Packages.

UNIT II

BUILDING SIMULATION MODELS: Guidelines for Determining Levels of Model Detail, Techniques for Increasing Model Validity and Credibility.

MODELING TIME DRIVEN SYSTEMS: Modeling Input Signals, Delays, System Integration, Linear Systems, Motion Control Models, Numerical Experimentation.

UNIT III

EXOGENOUS SIGNALS AND EVENTS: Disturbance Signals, State Machines, Petri Nets & Analysis, System Encapsulation.

MARKOV PROCESS: Probabilistic Systems, Discrete Time Markov Processes, Random Walks, Poisson Processes, the Exponential Distribution, Simulating a Poison Process, Continuous-Time Markov Processes.

UNIT IV

EVENT DRIVEN MODELS: Simulation Diagrams, Queuing Theory, Simulating Queuing Systems, Types of Queues, Multiple Servers.

UNIT V

SYSTEM OPTIMIZATION: System Identification, Searches, Alpha/Beta Trackers, Multidimensional Optimization, Modeling and Simulation Mythology.

TEXT BOOKS:

1. *System Modeling & Simulation, an Introduction*, Frank L. Severance, John Wiley & Sons, 2001.
2. *Simulation Modeling and Analysis*, Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFERENCES:

1. *Systems Simulation*, Geoffrey Gordon, PHI, 1978.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4101) EMBEDDED SYSTEM DESIGN
(Common to VLSI & ES)
(Program Elective -I)

I M. Tech -I Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT-I

INTRODUCTION: Embedded System Overview, Embedded Hardware Units, Embedded Software in a System, Embedded System on Chip (SoC), Design Process, Classification of Embedded Systems.

UNIT-II

EMBEDDED COMPUTING PLATFORM: CPU Bus, Memory Devices, Component Interfacing, Networks for Embedded Systems, Communication Interfacings: RS232/UART, RS422/RS485, IEEE 488 Bus.

SURVEY OF SOFTWARE ARCHITECTURE: Round Robin, Round Robin with Interrupts, Function Queue Scheduling Architecture, Selecting an Architecture Saving Memory Space.

UNIT-III

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and Target Machines, Linkers, Locations for Embedded Software, Getting Embedded Software into Target System, Debugging Technique

RTOS CONCEPTS: Architecture of The Kernel, Interrupt Service Routines, Semaphores, Message Queues, Pipes

UNIT-IV

INSTRUCTION SETS: Introduction, Preliminaries, ARM Processor, SHARC Processor.

SYSTEM DESIGN TECHNIQUES: Design Methodologies, Requirement Analysis, Specifications, System Analysis and Architecture Design

UNIT-V

DESIGN EXAMPLES: Telephone PBX, Ink Jet Printer, Water Tank Monitoring System, GPRS, Personal Digital Assistants, Set Top boxes.

TEXT BOOKS:

1. *Computers as a component: principles of embedded computing system Design*-Wayne wolf
2. *An embedded software premier*: David E. Simon
3. *Embedded / real time systems*-KVKK Prasad, Dreamtech press, 2005

REFERENCES:

1. *Embedded real time systems programming*- Sriram V Iyer, Pankaj gupta, TMH, 2004
2. *Embedded system design* - A unified hardware/software introduction - Frank vahid, tony D.Givargis, John Willey, 2002

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4205) VERILOG HDL
(Program Elective -II)

I M. Tech -I Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT I

HARDWARE MODELING WITH THE VERILOG HDL: Hardware Encapsulation -The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behavioral Description in Verilog, Hierarchical Descriptions of Hardware, Structured (Top Down) Design Methodology, Arrays of Instances, Using Verilog for Synthesis, Language Conventions, Representation of Numbers.

UNIT II

LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOG HDL: User Defined Primitives – Combinational Behavior User-Defined Primitives –Sequential Behavior, Initialization of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings, Constants, Operators, Expressions and Operands, Operator Precedence Models of Propagation Delay: Built-In Constructs for Delay, Signal Transitions, Verilog Models for Gate Propagation Delay (Inertial Delay), Time Scales for Simulation, Verilog Models for Net Delay (Transport Delay), Module Paths and Delays, Path Delays and Simulation, Inertial Delay Effects and Pulse Rejection.

UNIT III

BEHAVIORAL DESCRIPTIONS IN VERILOG HDL: Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls and Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments and Ambiguity, Constructs for Activity Flow Control, Tasks and Functions, Summary of Delay Constructs in Verilog, System Tasks for Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models of Finite State Machines.

UNIT IV

SYNTHESIS OF COMBINATIONAL LOGIC: HDL-Based Synthesis, Technology-Independent Design, Benefits of Synthesis, Synthesis Methodology, Vendor Support, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three State Buffers, Synthesis of Sequential Logic: Synthesis of Sequential UDPs, Synthesis of Latches, Synthesis of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers and Counters, Synthesis of Finite State Machines.

SYNTHESIS OF LANGUAGE CONSTRUCTS: Synthesis of Nets, Synthesis of Register Variables, Restrictions on Synthesis of "X" and "Z", Synthesis of Expressions and Operators, Synthesis of Assignments, Synthesis of Case and Conditional Statement, Synthesis of Resets, Timings Controls in Synthesis, Synthesis of Multi-Cycle Operations, Synthesis of Loops, Synthesis if Fork Join Blocks, Synthesis of The Disable Statement Synthesis of User-Defined

Tasks, Synthesis of User-Defined Functions, Synthesis of Specify Blocks, Synthesis of Compiler Directives.

UNIT V

SWITCH-LEVEL MODELS IN VERILOG: MOS Transistor Technology, Switch Level Models of MOS Transistors, Switch Level Models of Static CMOS Circuits, Alternative Loads and Pull Gates, CMOS Transmission Gates, Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction by Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic, Design Examples in Verilog.

TEXT BOOKS:

1. *Modeling, Synthesis and Rapid Prototyping with the Verilog HDL*, M.D. CILETTI, Prentice-Hall, 1999.
2. *VHDL Analysis and Modeling of Digital Systems*, Z. NAWABI, (2/E), McGraw Hill, 1998.

REFERENCES:

1. *Verilog Digital – Computer Design*, M.G. ARNOLD, Prentice-Hall (PTR), 1999.
2. *VHDL*, PERRY, (3/E), McGraw Hill.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4206) ANALOG IC DESIGN
(Program Elective -II)

I M. Tech -I Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT I

INTEGRATED DEVICES AND MODELING AND CURRENT MIRROR: MOS Transistors- Modeling in Linear, Saturation and Cut Off High Frequency Equivalent Circuit. Advanced MOS Modeling, Large Signal and Small Signal Modeling for BJT/Basic Current Mirrors and Single Stage Amplifiers, Simple CMOS Current Mirror, High Output Impedance Current Mirrors and Bipolar Gain Stages, Frequency Response.

UNIT II

OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION: Two Stage CMOS Operational Amplifier, Feedback and Operational Amplifier Compensation, Advanced Current Mirror, Common Mode Feedback Circuits, Current Feedback Operational Amplifier, Comparator, Charge Injection Error, Latched Comparator and Bi-CMOS Comparators.

UNIT III

SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUITS-I: MOS, CMOS, Bi-CMOS Sample and Hold Circuits, Switched Capacitor Circuits, Basic Operation and Analysis. First Order and Biquard Filters.

SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUITS-II: Charge Injection. Switched Capacitor Gain Circuit, Correlated, Double Sampling Techniques, Other Switched Capacitor Circuits.

UNIT IV

DATA CONVERTERS: Ideal D/A & A/D Converters, Quantization Noise, Performance Limitations, Nyquist Rate D/A Converters: Decoders Based Converters. Binary Scaled Converters. Hybrid Converters. Nyquist Rate A/D Converters: Integrating, Successive Approximation, Cyclic Flash Type, Two Step, Interpolating, Folding and Pipelined, A/D Converters.

UNIT V

OVER SAMPLING CONVERTERS AND FILTERS: Over Sampling with and without Noise Shaping, Digital Decimation Filter, High Order Modulators, Band Pass Over Sampling Converter, Practical Considerations, And Continuous Time Filters.

TEXT BOOKS:

1. *Analog Integrated Circuit Design*, D.A. JOHN & KEN MARTIN, John Wiley, 1997.
2. *Design of Analog CMOS Integrated Circuit*, Behzad Razavi, Tata-Mc GrawHill, 2002.

REFERENCES:

1. *CMOS Analog Circuit Design*, Philip Allen & Douglas Holberg, Oxford Uiversity Press, 2002.
2. *Analog MOS Integrated Circuits*, John Wiley, 1986.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4015) IMAGE & VIDEO PROCESSING
(Common to VLSI & DECS)
(Program Elective -II)

I M. Tech –I Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT I

IMAGE REPRESENTATION: Gray Scale and Color Images, Image Sampling and Quantization. Two Dimensional Orthogonal Transforms: DFT, WT, Haar Transform, KLT, DCT.

UNIT II

IMAGE ENHANCEMENT: Filters in Spatial and Frequency Domains, Histogram-Based Processing and Homomorphic Filtering. Edge Detection, Non-Parametric and Model Based Approaches, LOG Filters, Localization Problem.

UNIT III

IMAGE RESTORATION: Degradation Models, PSF, Circulant And Block–Circulant Matrices, Deconvolution, Restoration Using Inverse Filtering, Wiener Filtering and Maximum Entropy-Based Methods, Morphological Operations.

IMAGE SEGMENTATION: Pixel Classification, Bi-Level Thresholding, Multi-Level Thresholding, P-Tile Method, Adaptive Thresholding, Spectral & Spatial Classification, Hough Transform, Region Growing.

UNIT IV

IMAGE COMPRESSION: Compression Models, Information Theoretic Perspective, Fundamental Coding Theorem.

LOSSLESS COMPRESSION: Huffman Coding, Arithmetic Coding, Bit Plane Coding, Run Length Coding, Lossy Compression: Transform Coding, Image Compression Standards.

UNIT V

VIDEO PROCESSING: Representation of Digital Video, Spatio-Temporal Sampling, Motion Estimation, Motion Compensation, Video Filtering, Video Compression, Video Coding Standards.

TEXT BOOKS:

1. *Digital Image Processing* R. C. Gonzalez, R. E. Woods, Pearson Education. 2nd edition, 2002
2. *Digital image processing*, W. K. Pratt, Prentice Hall, 1989
3. *Digital image processing*, A. Rosenfold and A. C. Kak, Vols. 1 and 2, Prentice Hall, 1986.

REFERENCES:

1. *Digital image restoration* H. C. Andrew and B. R. Hunt, Prentice Hall, 1977
2. *Machine Vision*, R. Jain, R.Kasturi and B.G.Schunck, McGraw-Hill International Edition, 1995.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4207) DIGITAL ELECTRONIC CIRCUITS LAB (VIRTUAL LAB)

I M. Tech -I Sem. (E.C.E) (VLSI)

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List of experiments:

1. Analysis of Functions of BCD-TO-7-segment Decoder / Driver and Operation of 7-Segment LED Display
2. Characterization of Digital Logic Families
3. Analysis and Synthesis of Boolean Expressions using Basic Logic Gates
4. Analysis and Synthesis of Logic Functions using Multiplexers
5. Analysis and Synthesis of Logic Functions using Decoders
6. Analysis and Synthesis of Boolean Relations using Digital Comparators
7. Analysis and Synthesis of Arithmetic Expressions using Adders / Subtractors
8. Analysis and Synthesis of Sequential Circuits using Basic Flip-Flops
9. Analysis and Synthesis of Multi-bit Sequential Circuits using Shift Registers
10. Design of Arithmetic Logic Unit (ALU)

Required Software Tools:

1. Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and above)
2. NgSpice Software tool

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4208) DIGITAL IC DESIGN LAB

I M. Tech -I Sem. (E.C.E) (VLSI)

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List of experiments:

1. Digital Circuits Description using Verilog and VHDL.
2. Verification of the Functionality of Designed Circuits using Function Simulator.
3. Timing Simulation for Critical Path Time Calculation.
4. Synthesis of Digital circuits.
5. Place and Route Techniques for Major FPGA Vendors such as Xilinx, Altera and Acteletc.
6. Implementation of Designed Digital Circuits using FPGA and CPLD devices.

Required Software Tools:

1. Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)
2. Xilinx 11.1i and Above for FPGA/CPLDS / FPGA Advantage

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18HS0823) RESEARCH METHODOLOGY AND IPR

I M.Tech -I Sem. (E.C.E) (VLSI)

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Course outcomes:

At the end of this course, students will be able to

- Understand research problem formulation. Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT I

Meaning of Research Problem, Sources of Research Problem, Criteria Characteristics of a Good Research Problem, Errors in Selecting a Research Problem, Scope and Objectives of Research Problem.

Approaches of Investigation of Solutions for Research Problem, Data Collection, Analysis, Interpretation, Necessary Instrumentations

UNIT II

Effective Literature Studies Approaches, Analysis Plagiarism, Research Ethics,

UNIT III

Effective Technical Writing, How to Write Report, Paper Developing a Research Proposal, Format of Research Proposal, a Presentation and Assessment by a Review Committee

UNIT IV

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: Technological Research, Innovation, Patenting, Development. International Scenario: International Cooperation on Intellectual Property. Procedure for Grants of Patents, Patenting Under PCT.

UNIT V

Patent Rights: Scope of Patent Rights. Licensing and Transfer of Technology. Patent Information and Databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New Developments in IPR, IPR of Biological Systems, Computer Software Etc. Traditional Knowledge Case Studies, IPR and IITS.

TEXT BOOKS:

1. *Research methodology: an introduction for science & engineering students,* Stuart Melville and Wayne Goddard.
2. *Research Methodology: An Introduction,* Wayne Goddard and Stuart Melville.
3. *Resisting Intellectual Property,* Ranjit Kumar, 2nd Edition, Research Methodology: A Step by Step Guide for beginners, Halbert,, Taylor & Francis Ltd ,2007.
4. *Industrial Design*, Mayall , McGraw Hill, 1992. Niebel ,"*Product Design*", McGraw Hill, 1974.
5. *Introduction to Design,* Asimov , Prentice Hall, 1962.
6. *Intellectual Property in New Technological Age,* Robert P. Merges, Peter S. Menell, Mark A. Lemley, 2016.
7. *Intellectual Property Rights Under WTO,* T. Ramappa, S. Chand, 2008

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18HS0818) ENGLISH FOR RESEARCH PAPER WRITING

I M.Tech -I Sem. (E.C.E) (VLSI)

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Course objectives:

Students will be able to:

1. Understand that how to improve your writing skills and level of readability.
2. Learn about what to write in each section.
3. Understand the skills needed when writing a Title.
4. Ensure the good quality of paper at very first-time submission.

UNIT I

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

UNIT II

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts and Introduction.

UNIT III

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT IV

Key Skills Needed When Writing a Title, Key Skills Needed When Writing Abstract, Key Skills Needed When Writing an Introduction, Skills When Writing a Review of the Literature.

UNIT V

Skills Needed When Writing the Methods, Skills Needed When Writing the Results, Skills Needed When Writing the Discussion, Skills Needed When Writing the Conclusions.

TEXT BOOKS:

1. *Writing for Science*, Goldbort R (2006), Yale University Press.
2. Day R (2006) *How to Write and Publish a Scientific Paper*, Cambridge University Press.
3. *Handbook of Writing for the Mathematical Sciences*, SIAM, Highman's Books, HighmanN (1998).
4. *English for Writing Research Papers*, Springer New York Dordrecht Heidelberg London, Adrian Wallwork, 2011.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18CE1029) DISASTER MANAGEMENT

I M.TECH - I SEM. (E.C.E) (VLSI)	**L**	**T**	**C**
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Course *Objective:*

The objectives of this subject is to give the basic knowledge of Environmental Hazards and disasters. The syllabus includes the basics of Endogenous and Exogenous hazards and gives a suitable picture on the different types of hazard and disaster mitigation methods.

Course Outcomes:

On completion of the course the students will have knowledge on

1. Types of disasters and their effects on environment
2. Causes of disasters
3. Disaster management through engineering applications

UNIT I

Environmental Hazards & Disasters: Meaning of Environmental Hazards, Environmental Disasters and Environmental Stress. Concept of Environmental Hazards, Environmental Stress & Environmental Disasters. Different Approaches & Relation With Human Ecology - Landscape Approach - Ecosystem Approach - Perception Approach - Human Ecology & its Application in Geographical Researches.

UNIT II

Types of Environmental Hazards & Disasters: Natural Hazards and Disasters – Man Induced Hazards & Disasters - Natural Hazards- Planetary Hazards/ Disasters – Extra Planetary Hazards/ Disasters - Planetary Hazards- Endogenous Hazards – Exogenous Hazards

UNIT III

Endogenous Hazards - Volcanic Eruption – Earthquakes – Landslides – Volcanic Hazards/ Disasters - Causes and Distribution of Volcanoes - Hazardous Effects of Volcanic Eruptions - Environmental Impacts of Volcanic Eruptions – Earthquake Hazards/ Disasters - Causes of Earthquakes - Distribution of Earthquakes – Hazardous Effects of - Earthquakes - Earthquake Hazards in India - - Human Adjustment, Perception & Mitigation of Earthquake.

UNIT IV

Exogenous Hazards/ Disasters - Infrequent Events- Cumulative Atmospheric Hazards/ Disasters Infrequent Events: Cyclones – Lightning – Hailstorms Cyclones: Tropical Cyclones & Local Storms - Destruction by Tropical Cyclones & Local Storms (Causes, Distribution Human Adjustment, Perception & Mitigation) Cumulative Atmospheric Hazards/ Disasters: - Floods- Droughts- Cold Waves- Heat Waves. Floods:- Causes of Floods- Flood Hazards India- Flood Control Measures (Human Adjustment, Perception & Mitigation).Droughts:- Impacts of Droughts- Drought Hazards in India- Drought Control Measures- Extra Planetary Hazards/ Disasters- Man Induced Hazards /Disasters- Physical Hazards/ Disasters-Soil Erosion Soil Erosion:-- Mechanics & Forms of Soil Erosion- Factors & Causes of Soil Erosion- Conservation Measures of Soil Erosion. Chemical Hazards/ Disasters: Release of

Toxic Chemicals, Nuclear Explosion- Sedimentation Processes. Sedimentation Processes: - Global Sedimentation Problems- Regional Sedimentation Problems- Sedimentation & Environmental Problems- Corrective Measures of Erosion & Sedimentation. Biological Hazards/ Disasters: - Population Explosion.

UNIT V

Emerging Approaches In Disaster Management- Three Stages

1. Pre- Disaster Stage (Preparedness)
2. Emergency Stage
3. Post Disaster Stage-Rehabilitation

TEXT BOOKS:

1. *Disaster Management*, Rajib Shah, Universities Press, India, 2003.
2. *Disaster Science and Management*, Tushar Bhattacharya, TMH Publications.
3. *Disaster Mitigation: Experiences and Reflections*, Pardeep Sahni.
4. *Natural Hazards & Disasters*, Donald Hyndman & David Hyndman – Cengage Learning

REFERENCES:

1. *The Environment as Hazards*, Kates, B.I & White, G.F, Oxford Publishers, New York, 1978
2. *Disaster Management*, R.B. Singh (Ed), Rawat Publication, New Delhi, 2000
3. *Disaster Management*, H.K. Gupta (Ed), Universiters Press, India, 2003
4. *Space Technology for Disaster Mitigation in India (INCED)*, R.B. Singh, University of Tokyo, 1994.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18HS0825) SANSKRIT FOR TECHNICAL KNOWLEDGE

I M.Tech -I Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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Course Objectives:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world.
- Learning of Sanskrit to improve brain functioning.
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects
- Enhancing the memory power.
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature.

Course Outcomes:

- Students will be able to
- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science & technology can be understood
- Being a logical language will help to develop logic in students

UNIT-I

Alphabets in Sanskrit, Past/Present/Future Tenses, Simple Sentences

UNIT-II

Order, Introduction of Roots, Technical Information about Sanskrit Literature

UNIT-III

Technical Concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TEXT BOOKS:

1. *Abhyaspustaka*, Dr.Vishwas, Samskrita-Bharti Publication, New Delhi
2. *Teach Yourself Sanskrit*, Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. *India's Glorious Scientific Tradition*, Suresh Soni, Ocean books (P) Ltd., New Delhi.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18HS0826) VALUE EDUCATION

I M. Tech. - I Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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Course Objectives:

Students will be able to

- Understand value of education and self- development
- Imbibe good values in students
- Let the should know about the importance of character

Course outcomes:

Students will be able to

- Knowledge of self-development.
- Learn the importance of Human values.
- Developing the overall personality.

UNIT I

Values and Self-Development – Social Values and Individual Attitudes. Work Ethics and Indian Vision of Humanism. Moral and Non-Moral Valuation. Standards and Principles. Value Judgements.

UNIT II

Importance of Cultivation of Values; Sense of Duty. Devotion, Self-Reliance; Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of Faith, National Unity. Patriotism. Love for Nature and Discipline.

UNIT III

- Personality and Behaviour Development - Soul and Scientific Attitude. Positive Thinking. Integrity and Discipline
- Punctuality, Love and Kindness.
- Avoid Fault Thinking.
- Free From Anger, Dignity of Labour.
- Universal Brotherhood and Religious Tolerance.
- True Friendship.
- Happiness Vs Suffering, Love for Truth.
- Aware of Self-Destructive Habits.
- Association and Cooperation.
- Doing Best for Saving Nature

UNIT IV

- Character and Competence –Holy Books Vs. Blind Faith.
- Self-Management and Good Health.
- Science of Reincarnation.
- Equality, Nonviolence, Humility, Role of Women.

- All Religions and Same Message.
- Mind Your Mind, Self-Control.
- Honesty, Studying Effectively.

TEXT BOOKS:

1. *Values and Ethics for organizations Theory and practice*, Chakroborty, S.K, Oxford University Press, New Delhi.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4209) FPGA ARCHITECTURES & APPLICATIONS
(Common to VLSI & ES)

I M. Tech -II Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT I

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice PLSI's Architectures – 3000 Series – Speed Performance and in System Programmability.

UNIT II

FPGA: Field Programmable Gate Arrays – Programming Technologies, Logic Blocks, Routing Architecture, Design Flow, Technology Mapping for FPGAs.

CASE STUDIES: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and Their Speed Performance.

UNIT III

FINITE STATE MACHINES (FSM): Top Down Design – State Transition Table, State Assignments for FPGAs, Problem of Initial State Assignment for One Hot Encoding, Derivations of State Machine Charges.

REALIZATION OF STATE MACHINE: Charts with a PAL, Alternative Realization for State Machine Chart using Microprogramming, Linked State Machines. One – Hot State Machine, Petrinets for State Machines – Basic Concepts, Properties, Extended Petrinets for Parallel Controllers. Finite State Machine Case study, Meta Stability, Synchronization.

UNIT IV

FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN: Architectures Centered around Non-Registered PLDs. State Machine Designs Centered around Shift Registers, one – Hot Design Method, Use of ASMs in One – Hot Design, Application of One – Hot Method, System Level Design – Controller, Data Path and Functional Partition.

UNIT V

CASE STUDIES: Combinational Logic Circuits - Parallel Adder Cell, Parallel Adder Sequential Circuits - Decade Counters, Multipliers, Parallel Controller design.

TEXT BOOKS:

1. *Digital Design Using Field Programmable Gate Array,* P.K.Chan & S. Mourad, jPrentice Hall (Pte), 1994.

REFERENCES:

1. *Field Programmable Gate Array Technology,* S.Trimberger, Edr., Kluwer Academic Publications,1994.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4210) LOW POWER VLSI DESIGN

I M. Tech -II Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT I

LOW POWER DESIGN, AN OVER VIEW: Introduction to Low- Voltage Low Power Design, Limitations, Silicon-On-Insulator.

MOS/ BiCMOS PROCESSES: Bi-CMOS Processes, Integration and Isolation Considerations, Integrated Analog/Digital CMOS Process.

UNIT II

LOW-VOLTAGE/LOW POWER CMOS/ BiCMOS PROCESSES: Deep Submicron Processes, SOI CMOS, Lateral BJT on SOI, Future Trends and Directions Of CMOS/Bi-CMOS Processes.

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET Models, Limitations of MOSFET Models, Bipolar Models, Analytical and Experimental Characterization of Sub-Half Micron MOS Devices, MOSFET in A Hybrid Mode Environment.

UNIT III

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS Logic Gates, Performance Evaluation.

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of Advanced Bi-CMOS Digital Circuits, ESD-Free Bi-CMOS, Digital Circuit Operation and Comparative Evaluation.

UNIT IV

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip Flops-Quality Measures for Latches and Flip Flops, Design Perspective.

UNIT V

SPECIAL TECHNIQUES: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

TEXT BOOKS:

1. *CMOS/BiCMOS ULSI low voltage, low power*, Yeo Rofail/ Gohl (3 Authors), Pearson Education Asia 1st Indian reprint,2002.
2. *Practical Low Power Digital VLSI Design*, Gary K. Yeap, KAP, 2002.

REFERENCES:

1. *Basic VLSI Design*, Douglas A.Pucknell & Kamran Eshraghian, 3rd edition PHI.
2. *Digital Integrated circuits*, J.Rabaey, PH,1996.
3. *CMOS Digital ICs*, Sung-mo Kang and yusuf leblebici, 3rd edition TMH 2003.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4211) NANO ELECTRONICS
(Program Elective -III)

I M. Tech -II Sem. (E.C.E) (VLSI)

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UNIT I

TECHNOLOGY AND ANALYSIS: Film Deposition Methods, Lithography, Material Removing Technologies, Etching and Chemical, Mechanical Processing, Scanning Probe Techniques.

CARBON NANO STRUCTURES: Carbon Clusters, Carbon Nano tubes, Fabrication, Electrical, Mechanical and Vibrational Properties, Applications of Carbon Nano Tubes.

UNIT II

LOGIC DEVICES: Silicon MOSFETS, Novel Materials and Alternative Concepts, Ferro Electric Filed Effect Transistors, Super Conductor Digital Electronics, Carbon Nano Tubes for Data Processing.

UNIT III

RADOM ACESS MEMORIES: High Permittivity Materials for DRAMs, Ferro Electric Random-Access Memories, Magneto-Resistive RAM.

UNIT IV

MASS STORAGE DEVICES: Hard Disk Drives, Magneto Optical Disks, Rewriteable DVDs based on Phase Change Materials, Holographic Data Storage.

UNIT V

DATA TRANSIMISSION, INTERFACES AND DISPLAYS: Photonic Networks, Microwave Communication Systems, Liquid Crystal Displays, Organic Light Emitting Diodes.

TEXTBOOKS:

1. *Nano Electronics and Information Technology*, Rainer Waser, Wiley VCH, April 2003.
2. *Introduction to Nano Technology*, Charles Poole, Wiley Interscience, May 2003.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(18EC4212) ALGORITHMS FOR VLSI DESIGN AUTOMATION

I M. Tech -II Sem. (E.C.E) (VLSI)

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UNIT I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation Tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable problems.

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu Search, Genetic Algorithms.

UNIT II

Layout Compaction, Placement, Floor Planning and Routing Problems, Concepts and Algorithms.

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT III

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision Diagrams, Two-Level logic Synthesis.

UNIT IV

HIGH-LEVEL SYNTHESIS: Hardware Models, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some Aspects of Assignment problem, High-level Transformations.

UNIT V

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA Technologies, Physical Design Cycle for FPGA's, Partitioning and Routing for Segmented and Staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM Technologies, MCM Physical Design Cycle, Partitioning, Placement - Chip Array Based and Full Custom Approaches, Routing, Maze Routing, Multiple Stage Routing, Topologic Routing, Integrated Pin – Distribution and Routing, Routing and Programmable MCM's.

TEXTBOOKS:

1. *Algorithms for VLSI Design Automation*, S.H.Gerez, Wiley Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999.
2. *Algorithms for VLSI Physical Design Automation*, Naveed Sherwani, 3rd edition, Springer International Edition, 2005.

REFERENCES:

1. *Computer Aided Logical Design with Emphasis on VLSI*, Hill & Peterson, Wiley, 1993.
2. *Modern VLSI Design: Systems on silicon*, Wayne Wolf, Pearson Education Asia, 2nd Edition, 1998.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
(18EC4001) ADVANCED DIGITAL SYSTEM DESIGN
(Common to VLSI & DECS)

I M. Tech -II Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT I

DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware Description Language and Control Sequence Method, Reduction of State Tables, State Assignments.

SEQUENTIAL CIRCUIT DESIGN: Design of Iterative Circuits, Design of Sequential Circuits Using ROMs, PLAs, CPLD and FPGAs

UNIT II

FAULT MODELING: Fault Classes and Models – Stuck at Faults, Bridging Faults, Transition and Intermittent Faults.

TEST GENERATION: Fault Diagnosis of Combinational Circuits by Conventional Methods– Path Sensitization Technique, Boolean Difference Method, Kohavi Algorithm.

UNIT III

TEST PATTERN GENERATION: D – Algorithm, PODEM, Random testing, Transition Count Testing, Signature Analysis and Testing for bridging faults.

UNIT IV

PROGRAMMING LOGIC ARRAYS: Introduction, Design using PLA's, PLA Minimization and PLA Folding.

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State Identification and Fault Detection Experiment. Machine Identification, Design of Fault Detection Experiment.

UNIT V

PLA TESTING: Fault Models, Test generation and Testable PLA design.

ASYNCHRONOUS SEQUENTIAL MACHINE: Fundamental Mode Model, Flow Table, State Reduction, Minimal Closed Covers, Races, Cycles and Hazards.

TEXTBOOKS:

1. *Switching & finite Automata Theory,* Z. Kohavi (TMH)
2. *Logic Design Theory*, N. N. Biswas, – (PHI)
3. *Digital Logic Design Principles*, Nolman Balabanian, Bradley Calson Wily Student Edition 2004.

REFERENCES:

1. *Digital System Testing and Testable Design,* M. Abramovici, M. A. Breues, A. D. Friedman, Jaico Publications.
2. *Fundamentals of Logic Design*, Charles H. Roth Jr.
3. *Computer Aided Logic Design*, Frederick. J. Hill & Peterson, Wiley 4th Edition.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4213) TESTING & TESTABILITY
(Common to VLSI, DECS & ES)

I M. Tech -II Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT I

INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT) FUNDAMENTALS: Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models, Levels of Modeling, Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

UNIT II

FAULT MODELING: Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck – Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits.

TESTING FOR SINGLE STUCK FAULTS (SSF): Automated Test Pattern Generation (ATPG/ATG) For SSFs in Combinational and Sequential Circuits, Functional Testing with Specific Fault Models.

UNIT III

DESIGN FOR TESTABILITY: Testability Trade-Offs, Techniques, Scan Architectures and Testing – Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design, Board Level and System Level DFT Approaches, Boundary Scans Standards, Compression Techniques – Different Techniques, Syndrome Test and Signature Analysis.

UNIT IV

BUILT-IN SELF-TEST (BIST): BIST Concepts and Test Pattern Generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level.

UNIT V

MEMORY BIST (MBIST): Memory Test Architectures and Techniques – Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model. Memory Test Requirements for MBIST.

BRIEF IDEAS ON EMBEDDED CORE TESTING: Introduction to Automatic in Circuit Testing (ICT), JTAG Testing Features.

TEXT BOOKS:

1. *Digital Systems Testing and Testable Design*, Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Jaico Publishing House, 2001.

REFERENCES:

1. *Design for Test for Digital ICs & Embedded Core Systems*, Alfred Crouch, Prentice Hall.
2. *Introduction to VLSI Testing, Prentice Hall*, Englehood Cliffs, 1998. Robert J.Feugate, Jr., Steven M.Mentyn,

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4104) REAL TIME OPERATING SYSTEMS
(Common to VLSI & ES)

I M. Tech -II Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT I

OPERATING SYSTEMS: Overview, Time Services and Scheduling Mechanisms, other Basic Operating System Function, Processor Reserves and Resource Kernel. Capabilities of Commercial Real Time Operating Systems.

UNIT II

INTRODUCTION TO UNIX: Overview of Commands, File I/O. (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

UNIT III

REAL TIME SYSTEMS: Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources

UNIT IV

APPROACHES TO REAL TIME SCHEDULING: Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

FAULT TOLERANCE TECHNIQUES: Introduction, Fault Causes, Types, Detection, Fault and Error Containment, Redundancy: Hardware, Software, Time. Integrated Failure Handling.

UNIT V

CASE STUDIES-VX WORKS: Memory Managements Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches – Semaphore – Binary Mutex, Counting: Watch Dugs, I/O System

RT Linux: Process Management, Scheduling, Interrupt Management, and Synchronization

TEXT BOOKS:

1. *Advanced Unix Programming*, Richard Stevens.
2. *Real Time Systems*, Jane W.S. Liu Pearson Education.
3. *Real Time Systems*, C.M.Krishna, KANG G. Shin, McGraw. Hill.

REFERENCES:

1. Vx Works Programmers Guide.
2. www.tidp.org

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4214) SOLID STATE DEVICE MODELING AND SIMULATION
(Program Elective -IV)

I M. Tech -II Sem. (E.C.E) (VLSI)	L	T	C
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UNIT I

MOSFET DEVICE PHYSICS: MOSFET Capacitor, Basic Operation, Basic Modeling, Advanced MOSFET Modeling, RF Modeling of MOS Transistors, Equivalent Circuit Representation of MOS Transistor, High Frequency Behavior of MOS Transistor And A.C Small Signal Modeling, Model Parameter Extraction, Modeling Parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II

DEVICE MODELLING: Prime Importance of Circuit and Device Simulations In VLSI; Nodal, Mesh, Modified Nodal and Hybrid Analysis Equations. Solution of Network Equations: Sparse Matrix Techniques, Solution of Nonlinear Networks Through Newton-Raphson Technique, Convergence and Stability.

UNIT III

MULTISTEP METHODS: Solution of Stiff Systems of Equations, Adaptation of Multistep Methods to The Solution of Electrical Networks, General Purpose Circuit Simulators.

UNIT IV

MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS: Poisson Equation, Continuity Equation, Drift-Diffusion Equation, Schrodinger Equation, Hydrodynamic Equations, Trap Rate, Finite Difference Solutions to These Equations in 1D and 2D Space, Grid Generation.

UNIT V

SIMULATION OF DEVICES: Computation of Characteristics of Simple Devices Like P-N Junction, MOS Capacitor and MOSFET, Small-Signal Analysis.

TEXT BOOKS:

1. *MOSFET Models for VLSI Circuit Simulation,* Arora, N., Springer-Verlag, 1993
2. *Analysis and Simulation of Semiconductor Devices,* Selberherr, S., Springer-Verlag., 1984
3. *Introduction to Device Modeling and Circuit Simulation,* Wiley Fjeldly, T., Yetterdal, T. and Shur, M., -Interscience., 1997
4. *Advanced Device Modeling and Simulation Grasser,* T., World Scientific Publishing Company., 2003

REFERENCES:

1. *Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques,* Chua, L.O. and Lin, P.M., Prentice-Hall., 1975
2. *Device Modeling for Analog and RF CMOS Circuit Design,* Trond Ytterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf, John Wiley & Sons Ltd.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4215) MIXED SIGNAL LABORATORY

I M. Tech -II Sem. (E.C.E) (VLSI)

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List of experiments:

1. Analog Circuits Simulation using Spice.
2. Mixed Signal Simulation using Mixed Signal Simulators.
3. Layout Extraction for Analog & Mixed Signal Circuits.
4. Parasitic Values Estimation from Layout.
5. Layout Vs Schematic.
6. Net List Extraction.
7. Design Rule Checks.

Required Software Tools:

1. Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)
2. Xilinx 9.1i and Above for FPGA/CPLDS.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4216) DIGITAL VLSI DESIGN LAB (VIRTUAL LAB)

I M. Tech -II Sem. (E.C.E) (VLSI)

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List of experiments:

1. Plot the Output Characteristics & Transfer Characteristics of an n-channel and p-channel MOSFET.
2. Design and Plot the Static (VTC) and Dynamic Characteristics of a Digital CMOS Inverter.
3. Design and Plot the Output Characteristics of a 3-inverter Ring Oscillator.
4. Design and Plot the Dynamic Characteristics of 2-input NAND, NOR, XOR and XNOR Logic Gates using CMOS Technology.
5. Design and Plot the Characteristics of a 4x1 Digital Multiplexer using Pass Transistor Logic.
6. Design and Plot the Characteristics of a Positive and Negative Latch Based on Multiplexers.
7. Design and Plot the Characteristics of a Master-Slave Positive and Negative Edge Triggered Registers Based on Multiplexers.

Required Software Tools:

1. NgSpice Software tool

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18HS0829) CONSTITUTION OF INDIA

I M.Tech -II Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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Course Objectives:

Students will be able to

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals 'constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

UNIT I

History Of Making Of The Indian Constitution:

History, Drafting Committee, (Composition & Working)

UNIT II

Philosophy of The Indian Constitution: Preamble, Salient Features.

UNIT III

Contours of Constitutional Rights & Duties:

- Fundamental Rights
- Right to Equality
- Right to Freedom
- Right Against Exploitation
- Right to Freedom of Religion
- Cultural and Educational Rights
- Right to Constitutional Remedies
- Directive Principles of State Policy
- Fundamental Duties.

UNIT IV

Organs Of Governance:

- Parliament
- Composition
- Qualifications And Disqualifications
- Powers And Functions
- Executive
- President
- Governor
- Council of Ministers
- Judiciary, Appointment and Transfer of Judges, Qualifications

- Powers and Functions

UNIT V

Local Administration:

- District's Administration Head: Role and Importance,
- Municipalities: Introduction, Mayor and Role of Elected Representative, CEO of Municipal Corporation.
- Pachayati Raj: Introduction, PRI: Zila Pachayat.
- Elected Officials and Their Roles, CEO Zilapachayat: Position and Role.
- Block Level: Organizational Hierarchy (Different Departments),
- Village Level: Role of Elected and Appointed Officials,
- Importance of Grass Root Democracy.

Election Commission:

- Election Commission: Role and Functioning.
- Chief Election Commissioner and Election Commissioners.
- State Election Commission: Role and Functioning.
- Institute and Bodies for the Welfare of SC/ST/OBC and Women.

TEXT BOOKS:

1. *The Constitution of India*, 1950 (Bare Act), Government Publication.
2. F*raming of Indian Constitution,* Dr. S. N. Busi, Dr. B. R. Ambedkar, 1st Edition, 2015.
3. *Indian Constitution Law*, M. P. Jain, 7th Edn., Lexis Nexis, 2014.
4. *Introduction to the Constitution of India,* D.D. Basu, Lexis Nexis, 2015.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18HS0827) PEDAGOGY STUDIES

I M.Tech -II Sem. (E.C.E) (VLSI)

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Course Objectives:

Students Will Be Able To

- Review Existing Evidence On The Review Topic To Inform Programme Design And Policy
  Making Undertaken By The Dfid, Other Agencies And Researchers.
- Identify Critical Evidence Gaps To Guide The Development.

Course Outcomes

Students Will Be Able To Understand

- What Pedagogical Practices Are Being Used By Teachers In Formal And Informal Classrooms In Developing Countries?
- What Is The Evidence On The Effectiveness Of These Pedagogical Practices, In What Conditions, And With What Population Of Learners?
- How Can Teacher Education (Curriculum And Practicum) And The School Curriculum And Guidance Materials Best Support Effective Pedagogy?

UNIT I

Introduction And Methodology:

- Aims and Rationale, Policy Background, Conceptual Framework and Terminology.
- Theories of Learning, Curriculum, Teacher Education.
- Conceptual Framework, Research Questions**.**
- Overview of Methodology and Searching.

UNIT II

- Thematic Overview: Pedagogical Practices are Being Used by Teachers in Formal and Informal Classrooms in Developing Countries.
- Curriculum, Teacher Education.

UNIT III

- Evidence on the Effectiveness of Pedagogical Practices.
- Methodology for the in Depth Stage: Quality Assessment of Included Studies.
- How Can Teacher Education (Curriculum And Practicum) and the School Curriculum and Guidance Materials Best Support Effective Pedagogy?
- Theory of Change.
- Strength and Nature of the Body of Evidence for Effective Pedagogical Practices.
- Pedagogic Theory and Pedagogical Approaches.
- Teachers' Attitudes and Beliefs And Pedagogic Strategies.

UNIT IV

- Professional Development: Alignment with Classroom Practices and Follow-Up Support.
- Peer Support
- Support from the Head Teacher and the Community.
- Curriculum and Assessment
- Barriers to Learning: Limited Resources and Large Class Sizes

UNIT V

Research Gaps And Future Directions

- Research Design
- Contexts
- Pedagogy
- Teacher Education
- Curriculum and Assessment
- Dissemination asnd Research Impact.

TEXT BOOKS:

1. *Classroom Interaction In Kenyan Primary Schools,* Ackers J, Hardman F (2001) Compare, 31 (2): 245-261.
2. *The Importance Of Evaluation,* Agrawal M (2004) Curricular Reform In Schools: Journal Of Curriculum Studies, 36 (3): 361-379.
3. *Teacher Training In Ghana - Does It Count? Multi-Site Teacher Education Research Project (Muster) Country Report 1,* Akyeampong K (2003). London: Dfid.
4. *Improving Teaching And Learning Of Basic Maths And Reading In Africa: Does Teacher Preparation Count?,* Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) International Journal Educational Development, 33 (3): 272–282.
5. *International Comparisons In Primary Education. Oxford And Boston,* Alexander Rj (2001) Culture And Pedagogy, Blackwell.
6. *Learning To Read,* Chavan M (2003) Read India: A Mass Scale, Rapid, Campaign.
7. Www.Pratham.Org/Images/Resource%20working%20paper%202.Pdf.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18HS0828) STRESS MANAGEMENT BY YOGA

I M.Tech -II Sem. (E.C.E) (VLSI)

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Course Objectives:

- To Achieve Overall Health Of Body And Mind
- To Overcome Stress

Course Outcomes:

Students Will Be Able To

- Develop Healthy Mind In A Healthy Body Thus Improving Social Health Also
- Improve Efficiency.

UNIT I

Definitions of Eight Parts of Yoga (Ashtanga)

UNIT II

Yam and Niyam. Do`S and Don'ts in Life:
Ahinsa, Satya, Astheya, Bramhacharya and Aparigraha.
Shaucha, Santosh, Tapa, Swadhyay, Ishwarpranidhan.

UNIT III

Asan and Pranayam:
Various Yog Poses and Their Benefits for Mind & Body.
Regularization of Breathing Techniques and its Effects-Type of Pranayam.

TEXT BOOKS:

1. *Yogic Asanas For Group Tarining-Part-I*", Janardan Swami Yogabhyasi Mandal, Nagpur Model Curriculum Of Engineering & Technology Pg Courses [Volume-I] [47].
2. *Rajayoga Or Conquering The Internal Nature*, Swami Vivekananda, Advaitaashrama (Publication Department) Kolkata.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY: PUTTUR
(AUTONOMOUS)

(18HS0819) PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

I M.Tech -II Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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Course Objectives:

- To Learn To Achieve The Highest Goal Happily.
- To Become A Person With Stable Mind, Pleasing Personality And Determination.
- To Awaken Wisdom In Students.

Course Outcomes

Students Will Be Able To

- Study Of Shrimad-Bhagwad-Geeta Will Help The Student In Developing His Personality And Achieve The Highest Goal In Life.
- The Person Who Has Studied Geeta Will Lead The Nation And Mankind To Peace And Prosperity.
- Study Of Neetishatakam Will Help In Developing Versatile Personality Of Students.

UNIT I

Neetisatakam-Holistic Development Of Personality

- Verses- 19,20,21,22 (Wisdom)
- Verses- 29,31,32 (Pride & Heroism)
- Verses- 26,28,63,65 (Virtue)
- Verses- 52,53,59 (Dont's)
- Verses- 71,73,75,78 (Do's)

UNIT II

- Approach to Day to Day Work and Duties.
- Shrimad Bhagwadgeeta : Chapter 2-Verses 41, 47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

UNIT III

- Statements of Basic Knowledge.
- Shrimad Bhagwadgeeta: Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18
- Personality Of Role Model. Shrimad Bhagwadgeeta: Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

TEXT BOOKS:

1. *Srimad Bhagavad Gita*, Swami Swarupanandaadvaita Ashram (Publication Department), Kolkata.
2. *Bhartrihari's Three Satakam (Niti-Sringar-Vairagya)*, P.Gopinath, 4. Rashtriya Sanskrit Sansthanam, New Delhi.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4218) SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION

II M. Tech -I Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT-I

JavaScript – Object Models, Design Philosophy, Versions of JavaScript, The Java Script Core Language, Basic Concepts of Python. Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

UNIT-II

Overview of scripting language: PERL, File Handles, Operators, Control Structures, Regular Expressions, Built in Data Types, Operators, Statements and Declarations- Simple, Compound, Loop Statements, Global and Scoped Declarations.

UNIT-III

Pattern matching: Regular Expression, Pattern Matching Operators, Character Classes, Positions, Capturing and Clustering.

UNIT-IV

PERL Built-In Functions, Collections of Data, Working with Arrays, Lists and Hashes, Simple Input and Output, Strings, Patterns and Regular Expressions, Subroutines, Scripts with Arguments.

UNIT-V

Threads: Process Model, Thread Model, Perl Debugger, Using Debugger Commands, Customization, Internals and Externals, Internal Data Types, Extending Perl, Embedding Perl, Exercises for Programming Using Perl.

TEXT BOOKS:

1. *Learning PER*L, Randal L, Schwartz Tom Phoenix, Oreilly Publications, 3rd Edn., 2000
2. *Programming PERL*, Larry Wall, Tom Christiansen, John Orwant, Oreilly Publications, 3rd Edn., 2000.
3. *Java the Complete Reference*, Herbert Schildt, 7th Edition, TMH

REFERENCE BOOKS:

1. *The World of Scripting Languages,* David Barron, Wiley Student Edition, 2010

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4219) NANO MATERIALS AND TECHNOLOGY
(Program Elective -V)

II M. Tech -I Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT I

SEMICONDUCTOR NANOSTRUCTURES: Semiconductor Fabrication Techniques. Electronic Structure and Properties of Semiconductor Nanostructures. Principles and Performance of Semiconductor Nanostructures Based Electronic and Electro-Optical Devices.

UNIT II

MAGNETIC NANOSTRUCTURES: Magnetism in Solids-Magnetic Domains. Nano Magnetic Properties of Materials-Nanostructure Relationships. Fabrication and Properties of Nanostructured Magnets. Photo Induced Magnetism and Spintronic. Nano Magnetic Probes. Electronic Magneto Transport and Micro Magnetic Modeling.

UNIT III

NANOSENSORS AND ACTUATORS: Micro and Nano Electromechanical Systems-Fabrication Process, Choice of Materials, Calculations, Performance of Different Nanostructures, Advantages and Limitations of Various Approaches. Applications-Thermal, Radiation Magnetic, Chemical and Mechanical Nano Sensors and Micro Actuators.

UNIT IV

MOLECULAR ELECTRONICS: Conducting and Semiconducting Polymers-Hybridization, Conjugation and Excitations. Molecular Crystals. Organic Electroluminescent Displays-Injection, Transport, Exciton Formation and Light Emission. Influence of Supramolecular Order- Excimers, H and J Aggregates. Liquid Crystal Display.

UNIT V

INDUSTRIAL APPLICATIONS: Nanomaterials in Bone Substitutes & Dentistry. Antimicrobial Applications of Nanomaterials. Food and Cosmetic Applications of Nanomaterials. Application of Nanomaterials in Textiles, Paints, Catalysis, Lubricants, Fuel Cells and Batteries.

TEXT BOOKS:

1. *Laser Electronics*, J. Verdeyen, II Edition, Prentice Hall, 1990.
2. *Principles of Superconductive Devices and Circuits*, C.W. Turner, T. Van Duzer, 1981
3. *Electro responsive molecules and polymeric systems*, Reynolds, M.Pomeranty, Skotheim T. Marcel Dekker New York, 1991.

REFERENCES:

1. *Principles of Optical Electronics,* A. Yariv, John Wiley, New York, 1984
2. *Introduction to Molecular Electronics,* M C Petty, M R Bryce, D Bloor (eds.), Edward Arnold, London, 1995 (ISBN 0-340-58009-7)
3. *Semiconducting Polymers,* G Hadziioannou, P F van Hutten, Chemistry, Physics, and Engineering', Wiley-VCH, 2000 (ISBN 3-527-29507-0) 7 D. D. C Bradley, Current Opinion in Solid State & Materials Science Vol. 1, 789 (1996)

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EC4008) WIRELESS SENSOR NETWORKS
(Common to VLSI, DECS & ES)
(Program Elective -V)

II M. Tech.- I Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT I

Introduction and Overview of Sensor Network Architecture and Its Applications, Sensor Network Comparison with Adhoc Networks, Sensor Node Architecture with Hardware and Software Details.

UNIT II

Hardware: Examples Like Mica2, Micaz, Telosb, Cricket, Imote2, Tmote, Btnode, and Sun SPOT, Software (Operating Systems): Tinyos, MANTIS, Contiki and Retos. Programming Tools: C, Nesc. Performance Comparison of Wireless Sensor Networks Simulation and Experimental Platforms Like Open Source (Ns-2) And Commercial (Qualnet, Opnet)

UNIT III

Overview of Sensor Network Protocols (Details of Atleast 2 Important Protocol Per Layer): Physical, MAC and Routing/ Network Layer Protocols, Node Discovery Protocols, Multi-Hop and Cluster-Based Protocols, Fundamentals Of 802.15.4, Bluetooth, BLE (Bluetooth Low Energy), UWB.

UNIT IV

Data Dissemination and Processing; Differences Compared with Other Database Management Systems, Data Storage, Query Processing.

UNIT V

Specialized Features: Energy Preservation and Efficiency, Security Challenges, Fault Tolerance, Issues Related to Localization, Connectivity and Topology, Sensor Deployment Mechanisms, Coverage Issues, Sensor Web, Sensor Grid, Open Issues for Future Research, and Enabling Technologies in Wireless Sensor Network.

TEXT BOOKS:

1. *Protocols and Architectures for Wireless Sensor Networks*, H. Karl and A. Willig, John Wiley & Sons, India, 2012.
2. *Wireless Sensor Networks*, C. S. Raghavendra, K. M. Sivalingam, and T. Znati, Editors, Springer Verlag, 1st Indian reprint, 2010.

REFERENCE BOOKS:

1. *Wireless Sensor Networks, An Information Processing Approach* F. Zhao and L. Guibas, Morgan Kaufmann, 1st Indian reprint, 2013.
2. *Wireless sensor Network and Applications,* YingshuLi, MyT. Thai, Weili Wu, Springer series on signals and communication technology, 2008.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18HS0824) BUSINESS ANALYTICS
(Open Elective)

II M. Tech. - I Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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Course Objective:

The course is to understand the management and administration, functions of management, formal and informal organization, staffing, creativity and innovation, process of communication.

Course Outcomes:

CO -1: Design, device, and query relational databases for operative data.
CO - 2: Design, implement, populate and query data warehouses for informational data.
CO - 3: To integrate very large data sets to make business decisions.
CO - 4: Evaluate the use of data from acquisition through cleansing, warehousing, analytics, and visualization to the ultimate business decision.
CO - 5: Evaluate the key concepts of business analytics.
CO -6: Determine when to implement relational versus document-oriented database structures.
CO -7: Outline the relationship of the business analytics process within the organization's decision-making process.
CO - 8: Examine and apply appropriate business analytic techniques and methods.
CO–9: Execute real-time analytical methods on streaming datasets to react quickly to customer needs.
CO -10: To critically analyze the predictive analysis methods.

UNIT I

Introduction to Descriptive analytics, Descriptive Statistics, Probability Distributions, Inferential Statistics through hypothesis tests, Permutation & Randomization Test

UNIT II

Regression, ANOVA (Analysis of Variance), Machine Learning Introduction and Concepts Differentiating, algorithmic and model-based frameworks, Regression: Ordinary Least Squares, Ridge Regression, Lasso Regression, K Nearest Neighbors', Regression &Classification

UNIT III

Supervised Learning with Regression and Classification techniques- Bias-Variance Dichotomy, Model Validation Approaches, Logistic Regression, Linear Discriminant Analysis, Quadratic Discriminant Analysis, Regression and Classification Trees, Support Vector Machines, Ensemble Methods: Random Forest, Neural Networks, Deep learning

UNIT IV

Unsupervised Learning and Challenges for Big Data Analytics- Clustering, Associative Rule Mining, Challenges for big data analytics

UNIT V

Prescriptive analytics Creating data for analytics through designed experiments, creating data for analytics through Active learning, creating data for analytics through Reinforcement learning, Graph Visualization, Data Summaries, Model Checking & Comparison

TEXT BOOKS:

1. *The elements of statistical learning.Vol.2.No.1,* Hastie, Trevor, et al. New York: springer, 2009.
2. *Applied statistics and probability for engineers,* Montgomery, Douglas C., and George C. Runger. John Wiley & Sons, 2010
3. *Scaling up Machine Learning,* Bekkerman et al.
4. *Hadoop: The Definitive Guide*, Tom White Third Edition, O"reilly Media, 2012.
5. *Mining of Massive Datasets,* Anand Rajaraman and Jeffrey David Ullman, Cambridge University Press, 2012.
6. *Developing Analytic Talent: Becoming a Data Scientist*, Vincent Granville, wiley, 2014.
7. *Introduction to Data Science, Version 2.0,* Jeffrey Stanton & Robert De Graaf, 2013.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18ME3121) INDUSTRIAL SAFETY
(Open Elective)

II M.Tech -I Sem. (E.C.E) (VLSI)	**L**	**T**	**C**
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Course Objectives:

- *To learn about mechanical and electrical hazards.*
- *To learn about P mechanical and electrical hazards.*
- *To learn about Wear and Corrosion and their prevention.*
- *To learn about Periodic and preventive maintenance*

Course Outcomes:

Students undergoing this course are able to

- *Understand the points of factories act 1948 for health and safety.*
- *Understand the cost & its relation with replacement economy.*
- *Understand the concepts of sequence of fault finding activities*
- *Understand the Program and schedule of preventive maintenance of mechanical and electrical equipment.*

UNIT I

Industrial Safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc., Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT II

Fundamentals of Maintenance Engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT III

Wear and Corrosion and their Prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT IV

Fault Tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, Any one machine tool, Pump, Air compressor, Internal combustion engine, Boiler, Electrical motors, Types of faults in machine tools and their general causes.

UNIT-V

Periodic and Preventive Maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: Machine tools, Pumps, Air compressors, Diesel generating (DG) sets Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance.

Text Books:

1. *Maintenance Engineering Handbook,* Higgins & Morrow, Da Information Services, 2002
2. *Maintenance Engineering*, H. P. Garg, S. Chand and Company, 2008

Reference Books:

1. *Pump-hydraulic Compressors,* Audels, Mcgrew Hill Publication, 2009
2. *Foundation Engineering Handbook,* Winterkorn, Hans, Chapman & Hall London, 2010

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18ME3122) ADVANCED OPERATIONS RESEARCH
(Open Elective)

II M.Tech -I Sem. (E.C.E) (VLSI)

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Course Objectives:

- *To learn about Optimization Techniques.*
- *To learn about Graphical solution revised simplex method*
- *To learn about Nonlinear programming problem.*
- *To learn about Scheduling and sequencing and Competitive Models*

Course Outcomes:

Students undergoing this course are able to

- *Understand the Inventory Control Models*
- *Understand the Graphical solution revised simplex method*
- *Understand the concepts of Kuhn-Tucker conditions min cost flow.*
- *Understand the Probabilistic inventory control models and Dynamic Programming*

UNIT I

Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models.

UNIT II

Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming.

UNIT III

Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT.

UNIT IV

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

UNIT V

Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation.

Text Books:

1. *Operations Research, An Introduction*, H.A. Taha, PHI, 2008
2. *Principles of Operations Research*, H.M. Wagner, PHI, Delhi, 1982.
3. *Introduction to Optimization: Operations Research*, J.C. Pant, Jain Brothers, Delhi, 2008

Reference Books:

1. *Operations Research*: Hitler Liebermann McGraw Hill Pub. 2009
2. *Operations Research*: Pannerselvam, Prentice Hall of India 2010

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18CE1028) COST MANAGEMENT OF ENGINEERING PROJECTS
(Open Elective)

II M.TECH - I SEM. (E.C.E) (VLSI)	**L**	**T**	**C**
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Course Objectives:

- To study fundamentals of engineering project economics
- To understand dynamics of money over time
- To understand the significance of Benefit & Cost Analysis
- To get familiarised with depreciation, inflation and taxes
- To know the procedures of equipment costing
- To understand the basic concepts of Financial Management

Course Outcomes:

- Student can access the present value and future value for money
- Student can apply the principals of Benefit & Cost Analysis and
- Break-Even comparison
- Student can calculate the depreciation cost for construction equipment and can estimate the cost for construction equipment
- Can prepare profit and loss, balance sheets etc.

UNIT I

Engineering economics : Basic principles – Time value of money, Quantifying alternatives for decision making, Cash flow diagrams, Equivalence- Single payment in the future (P/F, F/P), Present payment compared to uniform series payments (P/A, A/P), Future payment compared to uniform series payments (F/A, A/F), Arithmetic gradient, Geometric gradient.

UNIT II

Comparison of alternatives: Present, future and annual worth method of comparing alternatives, Rate of return, Incremental rate of return, Break-even comparisons, Capitalized cost analysis, Benefit-cost analysis.

UNIT III

Depreciation, Inflation and Taxes: Depreciation, Inflation, Taxes.

Equipment economics: Equipment costs, Ownership and operating costs, Buy/Rent/Lease options, Replacement analysis.

UNIT IV

Cost Estimating: Types of Estimates, Approximate estimates – Unit estimate, Factor estimate, Cost indexes, parametric estimate, and Life cycle cost.

UNIT V

Financial management: Construction accounting, Chart of Accounts, Financial statements – Profit and loss, Balance sheets, Financial ratios, Working capital management.

Text Books / Reference Books:

1. *Engineering Economy by* Blank, L. T. and Tarquin, A. Fourth Edition, WCB/McGraw-Hill, 1998.
2. *Fundamentals of Financial management by* Bose, D. C. 2nd ed., PHI, New Delhi, 2010.
3. *Fundamentals of Financial management by* Boyer, C. B. and Merzbach, U. C., 2nd ed., John Wiley & Sons, New York, 1989.

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18ME3123) COMPOSITE MATERIALS

(Open Elective)

II M.Tech -I Sem. (E.C.E) (VLSI)

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Course Objectives:

- *To learn about Classification and characteristics of Composite materials*
- *To learn about layup method and Mechanical Behavior of composites*
- *To learn about Manufacturing of Metal Matrix Composites and Manufacturing of Polymer Matrix Composites*
- *To learn about Laminar Failure Criteria and Laminate strength-ply discount truncated maximum strain criterion*

Course Outcomes:

Students undergoing this course are able to

- *Understand the need of composite materials.*
- *Understand the Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites.*
- *Understand the concepts of Manufacturing of Ceramic Matrix Composite and Metal Matrix Composite.*
- *Understand the various manufacturing method of composites.*

UNIT I

Introduction: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT II

Reinforcements: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

UNIT III

Manufacturing Of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

UNIT IV

Manufacturing Of Polymer Matrix Composites: Preparation of Moulding compounds and prepress – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

UNIT V

Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hydro thermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

Text Books:

1. *Material Science and Technology* – Vol 13 – Composites by R.W.Cahn – VCH, West Germany, 2003
2. *Materials Science and Engineering*, An introduction. WD Callister, Jr., Adapted by R. Bala Subramanian, John Wiley & Sons, NY, Indian edition, 2007.

References:

1. *Hand Book of Composite Materials*-ed-Lubin. 2010
2. *Composite Materials* – K.K.Chawla. 2009
3. *Composite Materials Science and Applications* – Deborah D.L. Chung, 2012
4. *Composite Materials Design and Applications* – Danial Gay, Suong V. Hoa, and Stephen W. Tasi, 2012

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

(18EE2128) WASTE TO ENERGY
(Open Elective)

II M.TECH - I SEM. (E.C.E) (VLSI)	**L**	**T**	**C**
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UNIT I

INTRODUCTION TO ENERGY FROM WASTE: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors.

UNIT II

BIOMASS PYROLYSIS: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods -Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT III

BIOMASS GASIFICATION: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers –Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT IV

BIOMASS COMBUTION: Biomass stoves – Improved chullahs, types, some exotic designs, fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT V

PROPERTIES OF BIOGAS (CALORIFIC VALUE AND COMPOSITION): Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion Biomass energy programme in India.

References:

1. *Non-Conventional Energy by* Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. *Biogas Technology - A Practical Hand Book by* Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. *Food, Feed and Fuel from Biomass by* Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.